DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

APPLICATIONS

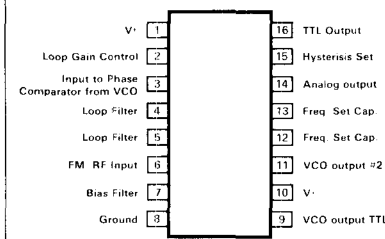
- **High speed modems**
- **FSK receivers and transmitters**
- ***Frequency synthesizers***
- **Signal generators**

FEATURES

- **Operation with single 5V supply**
- **TTL compatible inputs and outputs**
- **Operation to 50MHz**
- **Operates as a modulator**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**

PIN CONFIGURATION

N PACKAGE

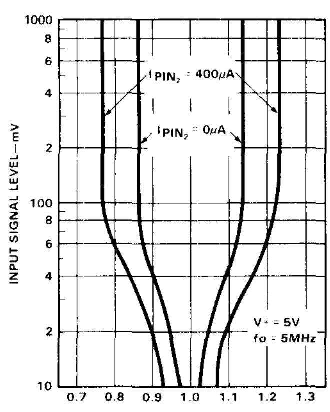


ABSOLUTE MAXIMUM RATINGS

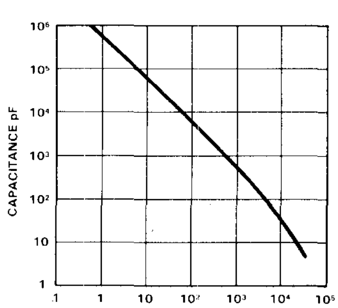
PARAMETER		RATING	UNIT
V+	Supply voltage		V
	Pin 1	14	
	Pin 10	6	
P_D	Power dissipation	400	mW
T_A	Operating temperature	0 to 70	°C
t_{stg}	Storage temperature	-65 to 150	°C

TYPICAL PERFORMANCE CHARACTERISTICS

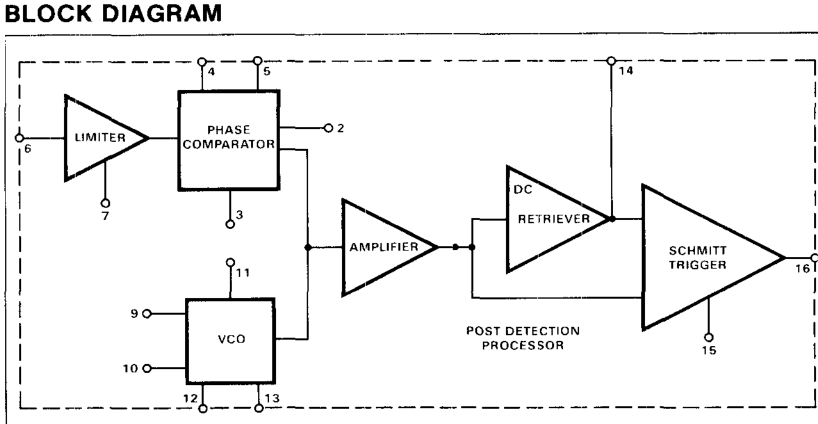
LOCK RANGE vs SIGNAL INPUT



VCO CAPACITOR vs FREQUENCY



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

Equation 1

$$v_o = \frac{(f_{in} - f_o)}{K_{VCO}}$$

K_{VCO} = conversion gain of the VCO
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into digital, logic compatible signals. For high data rates, a considerable amount of carrier

NE564-N

DC ELECTRICAL CHARACTERISTICS $V+ = 5V$, $T_A = 25°C$ unless otherwise specified

	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Lock range	$T_A = 25°C$, $I_2 = 400\mu A$	25	40		%
f_O	Frequency of operation of VCO		45	50		MHz
	Frequency drift with temperature	$T_A = 0°C$ to $70°C$, $f_O = 5MHz$		400	850	ppm/°C
	Frequency change with supply voltage	$V+ = 4.5V$ to $5.5V$		3	6	%/V
	Demodulated output voltage	± 1% input deviation	10	14		mVrms
		± 10% input deviation, $f_O = 5MHz$	100	140		
	Output voltage linearity			3		%
	Signal to noise ratio			40		dB
	AM rejection			35		dB
I_{CC}	Supply current	5V		30	40	mA
I_{LC}	Leakage current	Pin 9		1	10	μA
	Output current	Pin 9			6	mA
V+	Supply voltage	Pin 1	4.5		12	V
		Pin 10	4.5		5.5	

will be present at the output due to the the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources Q_{25}-Q_{26} form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

Equation 2

$$f_O = \frac{1}{16 R_C C_1}$$

$R_C = R_{19} = R_{20}$
C_1 = frequency setting external capacitor

Variation of V_d changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transconductance amplifier Q_{42}-Q_{43} with a capacitor at the output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

Equation 3

$$V_0 = \frac{g_m}{C_2} \int V_{in}\, dt$$

g_m = transconductance of the amplifier
C_2 = capacitor at the output (pin 14)
V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q_{49}-Q_{50} with positive feedback being provided by Q_{47}-Q_{48}. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

Free running frequency of VCO is shown by the following equation:

Equation 4

$$f_O = \frac{1}{16 R_C C_1} \text{ in Hz}$$

$R_C = 100\Omega$
C_1 = external cap in farads

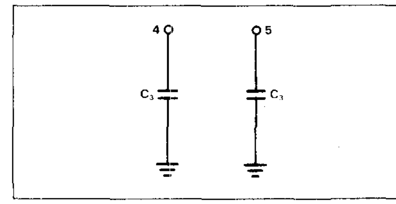
The loop filter diagram shown is explained by the following equation:

Equation 5

$$F(s) = \frac{1}{1 + sRC_3}$$

$R = R_{12} = R_{13} = 1.3k\Omega$

LOOP FILTER



EQUIVALENT SCHEMATIC