

MM54HCT573/MM74HCT573 TRI-STATE® Octal D-Type Latch MM54HCT574/MM74HCT574 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54HCT573/MM74HCT573 octal D-type latches and MM54HCT574/MM74HCT574 Octal D-type flip flops advanced silicon-gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The TRI-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT573/MM74HCT573 LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT574/MM74HCT574 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on

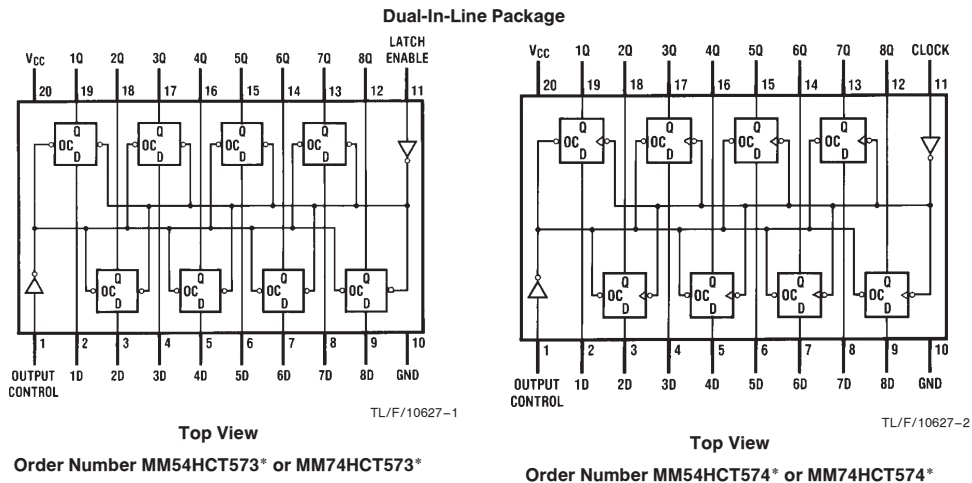
positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 18 ns
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	−0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC}=5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		74HCT	54HCT	Units
			Typ	T _A = −40 to 85°C			
V _{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V _{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA I _{OUT} = 6.0 mA, V _{CC} = 4.5V I _{OUT} = 7.2 mA, V _{CC} = 5.5V	V _{CC} 4.2 5.7	V _{CC} −0.1 3.98 4.98	V _{CC} −0.1 3.84 4.84	V _{CC} −0.1 3.7 4.7	V V V
V _{OL}	Maximum Low Level Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA I _{OUT} = 6.0 mA, V _{CC} = 4.5V I _{OUT} = 7.2 mA, V _{CC} = 5.5V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}		±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum TRI-STATE Output Leakage Current	V _{OUT} = V _{CC} or GND Enable = V _{IH} or V _{IL}		±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA		8.0	80	160	μA
		V _{IN} = 2.4V or 0.5V (Note 4)		1.5	1.8	2.0	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic “N” package: −12 mW/°C from 65°C to 85°C; ceramic “J” package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT573/MM74HCT573

$V_{CC} = 5.0V$, $t_r = t_f = 6$ ns $T_A = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay Data to Output	$C_L = 45$ pF	17	27	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L = 45$ pF	16	27	ns
t_{PZH} , t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L = 45$ pF $R_L = 1$ k Ω	21	30	ns
t_{PHZ} , t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L = 5$ pF $R_L = 1$ k Ω	14	23	ns
t_W	Minimum Clock Pulse Width			15	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			12	ns

AC Electrical Characteristics MM54HCT573/MM74HCT573

$V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		74HCT	54HCT	Units
					T _A = −40 to 85°C	T _A = −55 to 125°C	
			Typ	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay Data to Output	C _L = 50 pF	18	30	38	45	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Latch Enable to Output	C _L = 50 pF	17	30	44	53	ns
t _{PZH} , t _{PZL}	Maximum Enable Propagation Delay Control to Output	C _L = 50 pF R _L = 1 kΩ	22	30	38	45	ns
t _{PHZ} , t _{PLZ}	Maximum Disable Propagation Delay Control to Output	C _L = 50 pF R _L = 1 kΩ	15	30	38	45	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time	C _L = 50 pF	6	12	15	18	ns
t _W	Minimum Clock Pulse Width			15	20	24	ns
t _S	Minimum Setup Time Data to Clock		−3	5	6	8	ns
t _H	Minimum Hold Time Clock to Data		4	12	15	18	ns
C _{IN}	Maximum Input Capacitance			10	10	10	pF
C _{OUT}	Maximum Output Capacitance			20	20	20	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	OC = V _{CC} OC = GND		5 52			pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table

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Output Control	LE	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

'HCT574

Output Control	Clock	Data	Output
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level

X = Don't Care

$\uparrow$ = Transition from low-to-high

Z = High impedance state

Q_0 = The level of the output before steady state input conditions were established.

AC Electrical Characteristics MM54HCT574/MM74HCT574

$V_{CC} = 5.0V$, $t_r = t_f = 6\text{ ns}$ $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		60	33	MHz
t_{PHL} , t_{PLH}	Maximum Propagation Delay to Output	$C_L = 45\text{ pF}$	17	27	ns
t_{PZH} , t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L = 45\text{ pF}$ $R_L = 1\text{ k}\Omega$	19	28	ns
t_{PHZ} , t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L = 5\text{ pF}$ $R_L = 1\text{ k}\Omega$	14	25	ns
t_W	Minimum Clock Pulse Width			15	ns
t_S	Minimum Setup Time Data to Clock			12	ns
t_H	Minimum Hold Time Clock to Data			5	ns

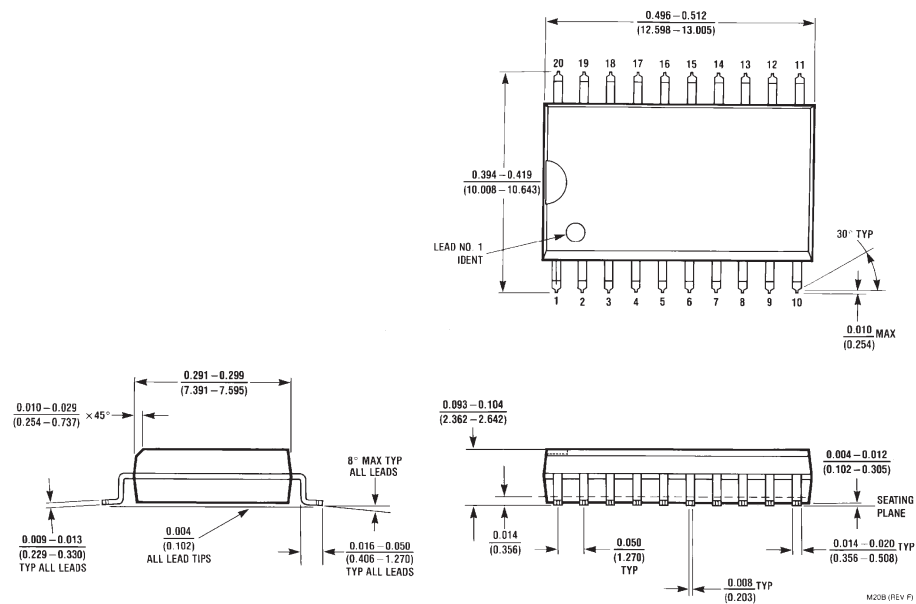
AC Electrical Characteristics MM54HCT574/MM74HCT574

$V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		74HCT	54HCT	Units
			Typ	Guaranteed Limits			
f _{MAX}	Maximum Clock Frequency			33	28	23	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay Clock to Output	C _L = 50 pF	18	30	38	45	ns
t _{PZH} , t _{PZL}	Maximum Enable Propagation Delay Control to Output	C _L = 50 pF R _L = 1 kΩ	22	30	38	45	ns
t _{PHZ} , t _{PLZ}	Maximum Disable Propagation Delay Control to Output	C _L = 50 pF R _L = 1 kΩ	15	30	38	45	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time	C _L = 50 pF	6	12	15	18	ns
t _W	Minimum Clock Pulse Width			15	20	24	ns
t _S	Minimum Setup Time Data to Clock		6	12	15	18	ns
t _H	Minimum Hold Time Clock to Data		−1	5	6	8	ns
C _{IN}	Maximum Input Capacitance			10	10	10	pF
C _{OUT}	Maximum Output Capacitance			20	20	20	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	OC = V _{CC} OC = GND		5 58			pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

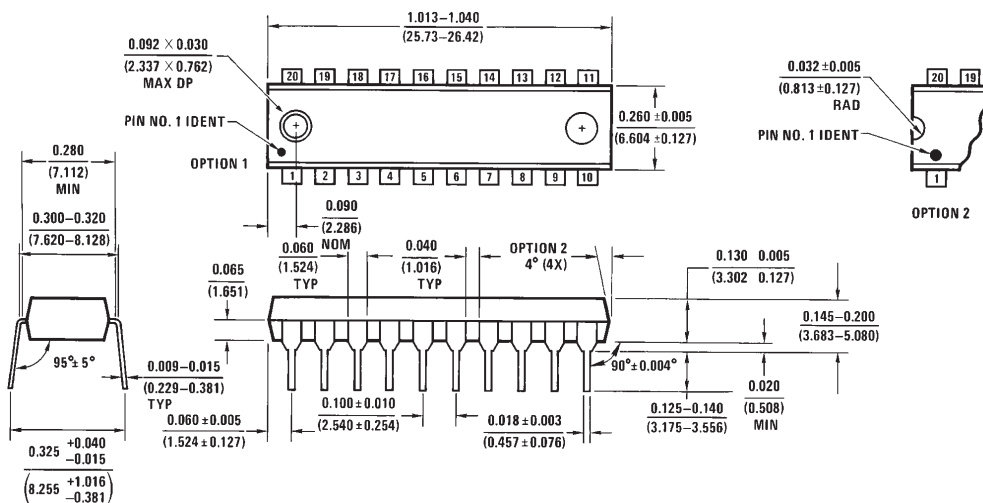
Physical Dimensions inches (millimeters)



Order Number MM74HCT573/HCT574 (WM)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

Lit. # 111670



Order Number MM74HCT573N/HCT574 (N)
NS Package Number N20A

N20A (REV G)

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

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