

Quad bistable transparent latch

74HC/HCT75

FEATURES

- Complementary Q and $\bar{Q}$ outputs
- V_{CC} and GND on the centre pins
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT75 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT75 have four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs (LE_{1-2} and LE_{3-4}). When LE_{n-n} is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LE_{n-n} is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LE_{n-n} will be stored in the latches. The latched outputs remain stable as long as the LE_{n-n} is LOW.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nD to nQ, $n\bar{Q}$	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	11	12	ns
	LE_{n-n} to nQ, $n\bar{Q}$		11	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	42	42	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 14, 11, 8	$1\bar{Q}$ to $4\bar{Q}$	complementary latch outputs
2, 3, 6, 7	1D to 4D	data inputs
4	LE_{3-4}	latch enable input, latches 3 and 4 (active HIGH)
5	V_{CC}	positive supply voltage
12	GND	ground (0 V)
13	LE_{1-2}	latch enable input, latches 1 and 2 (active HIGH)
16, 15, 10, 9	1Q to 4Q	latch outputs

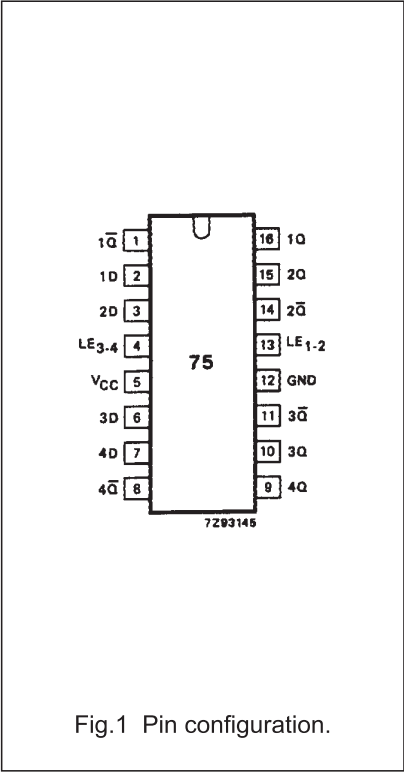


Fig.1 Pin configuration.

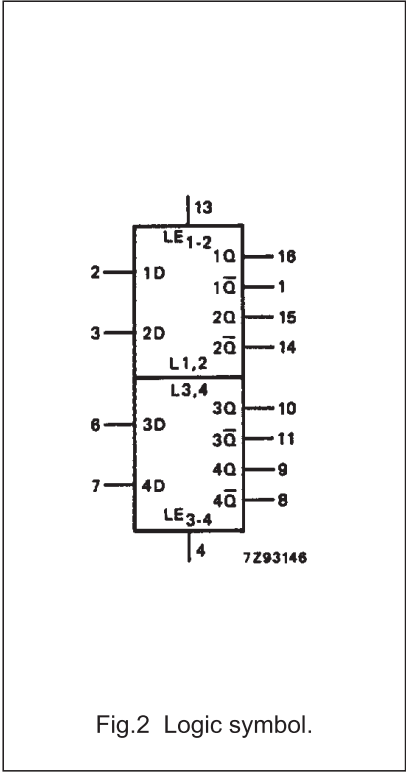


Fig.2 Logic symbol.

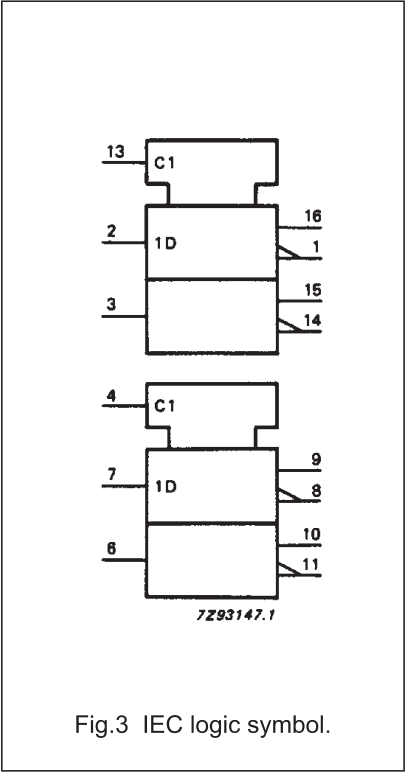


Fig.3 IEC logic symbol.

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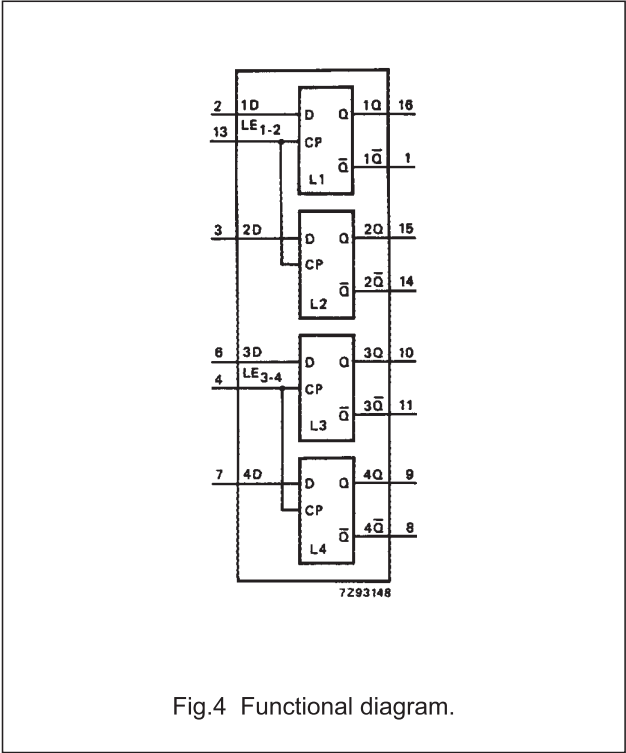
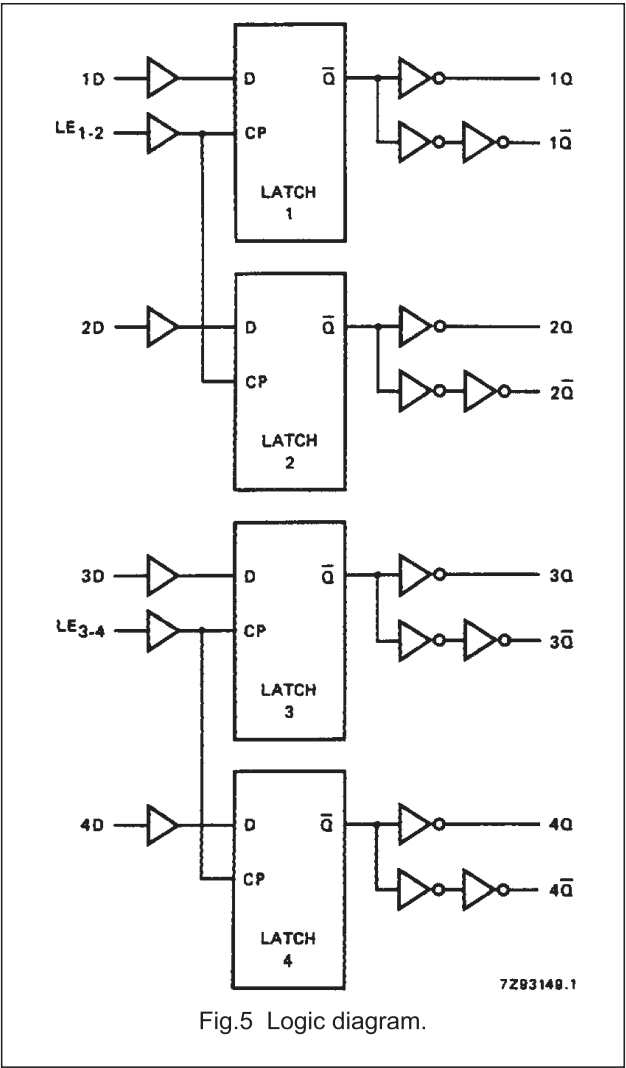
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FUNCTION TABLE

OPERATING MODES	INPUTS		OUTPUTS	
	LE _{n-n}	nD	nQ	nQ̄
data enabled	H	L	L	H
	H	H	H	L
data latched	L	X	q	q̄

Notes

1. H = HIGH voltage level
- L = LOW voltage level
- q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW LE_{n-n} transition
- X = don't care



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to+85		−40 to+125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay nD to nQ		33 12 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay nD to nQ̄		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay LE _{n-n} to nQ		33 12 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.8
t _{PHL} / t _{PLH}	propagation delay LE _{n-n} to nQ̄		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.8
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t _W	enable pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t _{su}	set-up time nD to LE _{n-n}	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.9
t _h	hold time nD to LE _{n-n}	3 3 3	−8 −3 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig.9

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nD	0.75
LE _{n-n}	1.00

AC CHARACTERISTICS FOR 74HCT

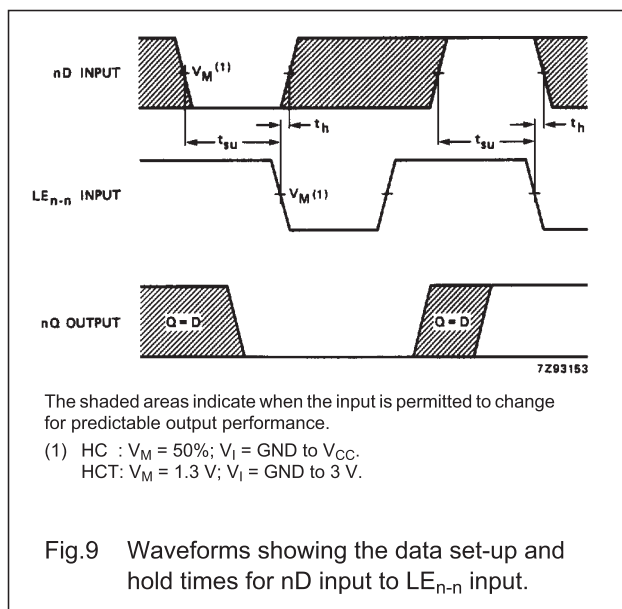
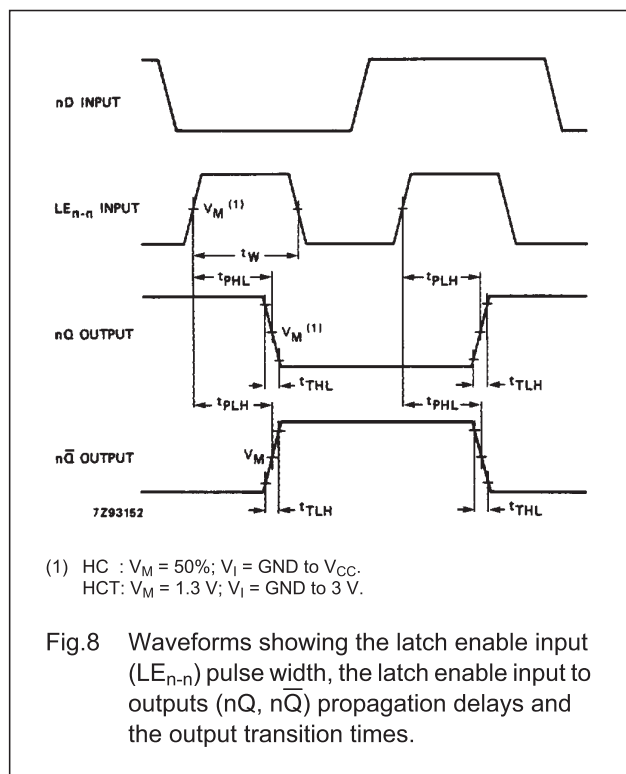
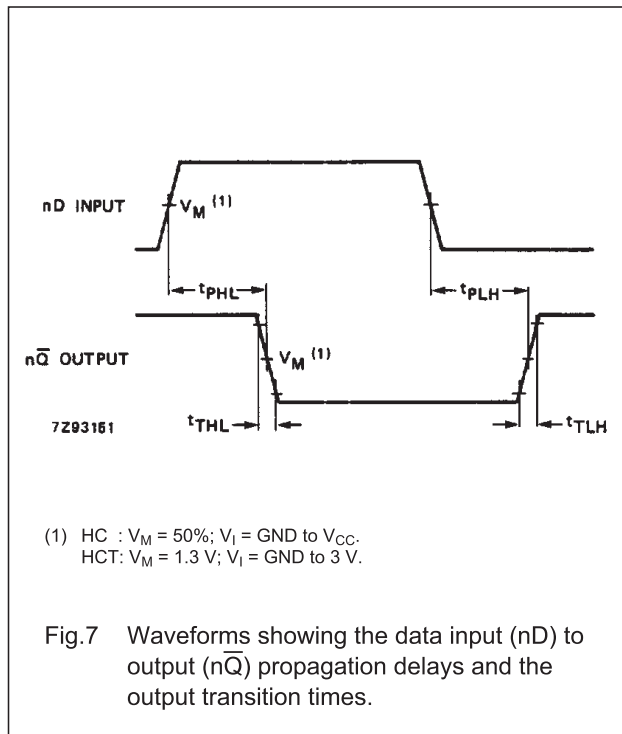
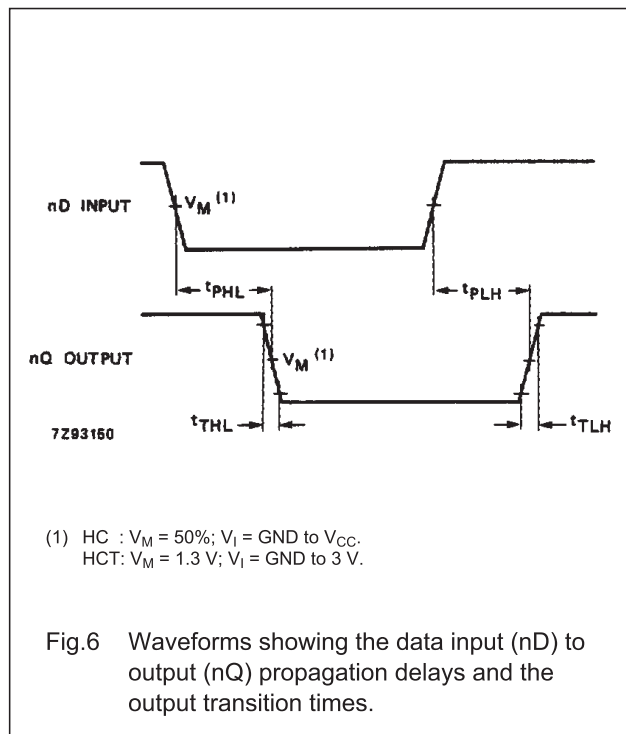
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay nD to nQ		15	28		35		42	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay nD to n $\overline{Q}$		15	28		35		42	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay LE _{n-n} to nQ		13	28		35		42	ns	4.5	Fig.8
t _{PHL} / t _{PLH}	propagation delay LE _{n-n} to n $\overline{Q}$		15	30		38		45	ns	4.5	Fig.8
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
t _W	enable pulse width HIGH	16	4		20		24		ns	4.5	Fig.8
t _{su}	set-up time nD to LE _{n-n}	12	4		15		18		ns	4.5	Fig.9
t _h	hold time nD to LE _{n-n}	3	−2		3		3		ns	4.5	Fig.9

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".