

Dual 4-channel analogue multiplexer/demultiplexer

HEF4052B
MSI

DESCRIPTION

The HEF4052B is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (Y_0 to Y_3) and a common input/output (Z). The common channel select logic includes two address inputs (A_0 and A_1) and an active LOW enable input ($\bar{E}$).

Both multiplexers/demultiplexers contain four bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_3) and the other side connected to a common input/output (Z).
With $\bar{E}$ LOW, one of the four switches is selected (low impedance ON-state) by A_0 and A_1 . With $\bar{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 and A_1 .

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 , A_1 and $\bar{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_3 , and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.
For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

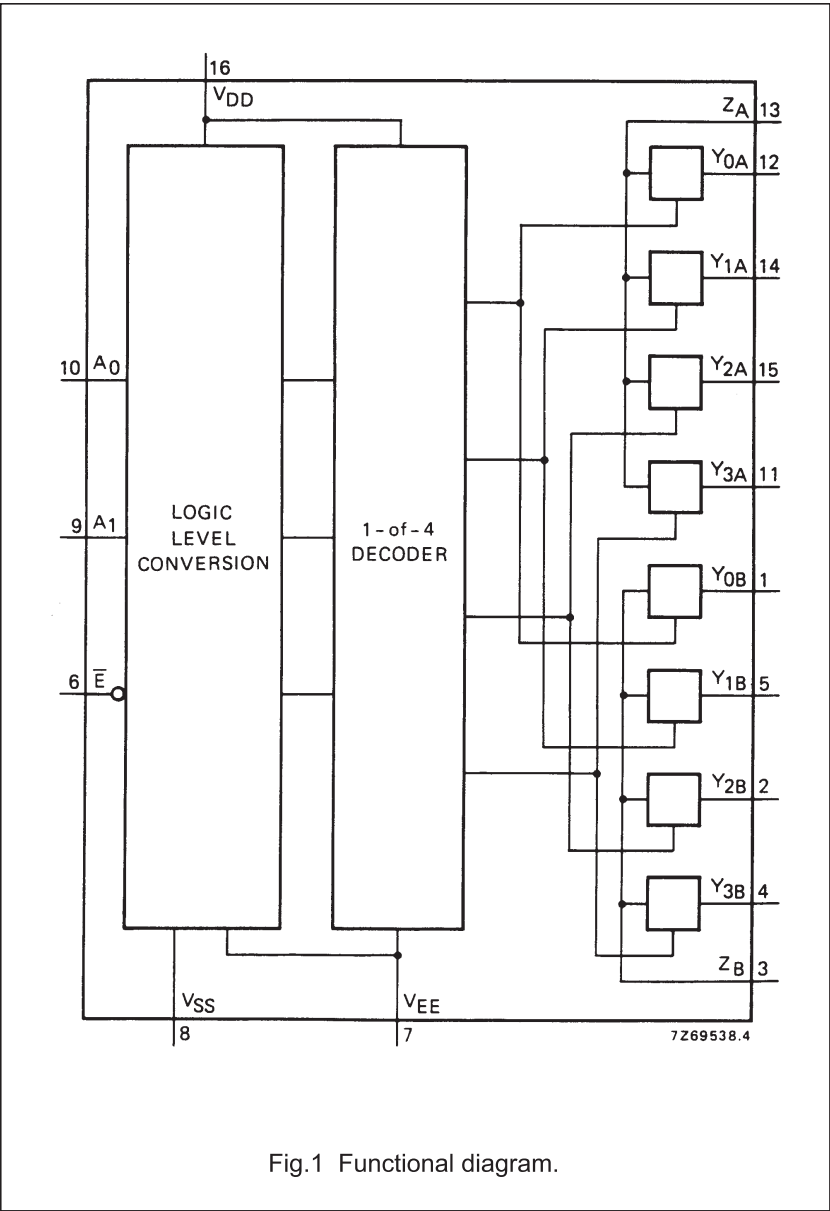


Fig.1 Functional diagram.

PINNING

- Y_{0A} to Y_{3A} independent inputs/outputs
- Y_{0B} to Y_{3B} independent inputs/outputs
- A_0 , A_1 address inputs
- $\bar{E}$ enable input (active LOW)
- Z_A , Z_B common inputs/outputs

FAMILY DATA,
 I_{DD} LIMITS category MSI
See Family Specifications

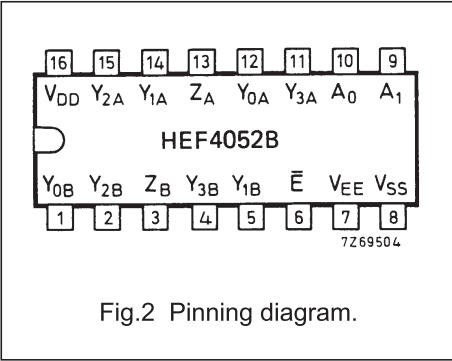
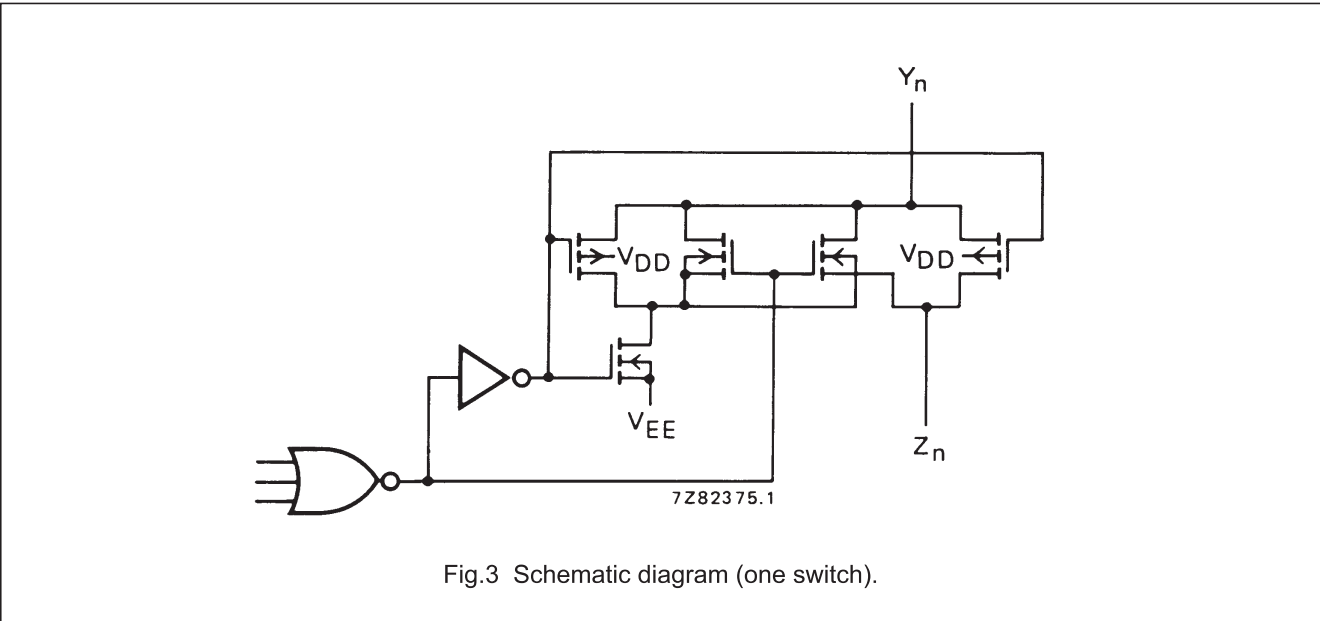


Fig.2 Pinning diagram.

- HEF4052BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4052BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4052BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

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FUNCTION TABLE

INPUTS			CHANNEL ON
$\bar{E}$	A_1	A_0	
L	L	L	$Y_{0A}-Z_A; Y_{0B}-Z_B$
L	L	H	$Y_{1A}-Z_A; Y_{1B}-Z_B$
L	H	L	$Y_{2A}-Z_A; Y_{2B}-Z_B$
L	H	H	$Y_{3A}-Z_A; Y_{3B}-Z_B$
H	X	X	none

Notes

- 1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

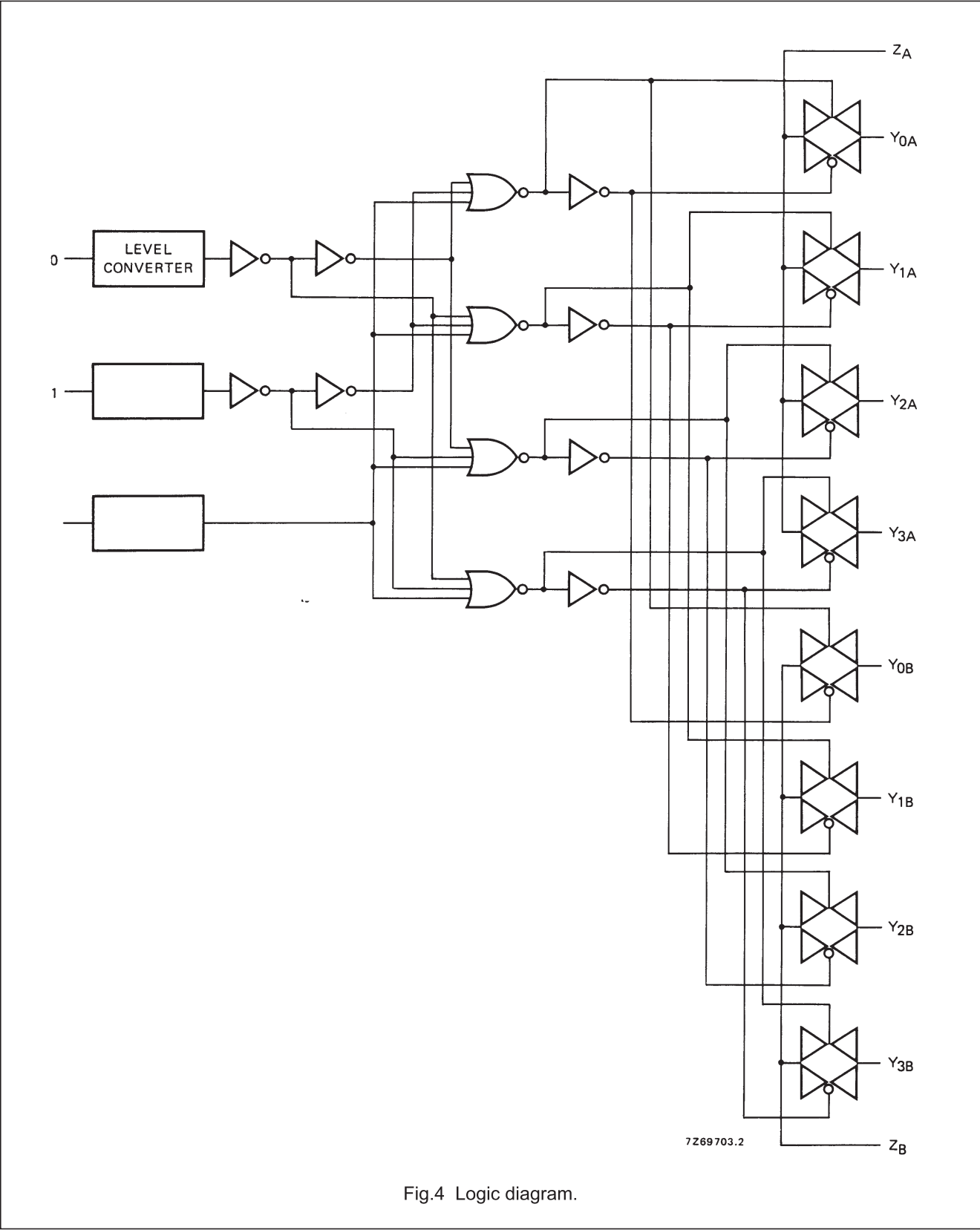
Supply voltage (with reference to V_{DD}) V_{EE} -18 to + 0,5 V

Note

- 1. To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE} .

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DC CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	SYMBOL	TYP.	MAX.		CONDITIONS
ON resistance	5	R_{ON}	350	2500	Ω	$V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig.6
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	$V_{is} = 0$ see Fig.6
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	$V_{is} = V_{DD}-V_{EE}$ see Fig.6
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	25	–	Ω	$V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig.6
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\bar{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\bar{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

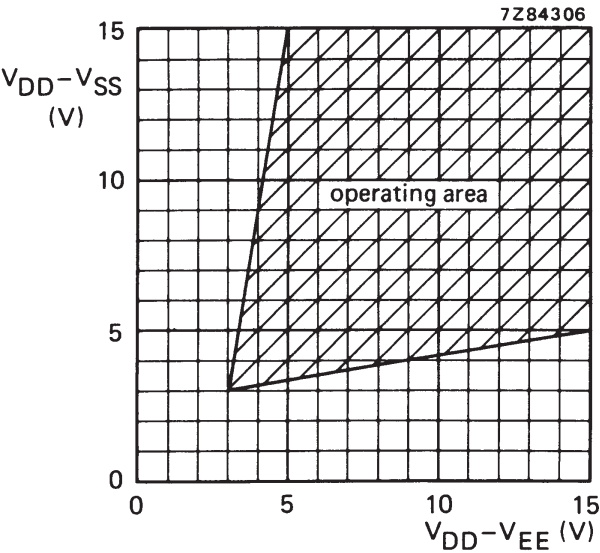
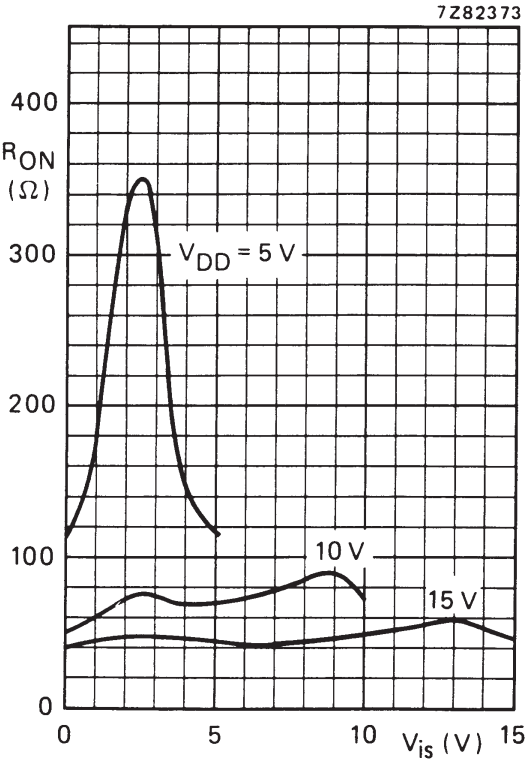
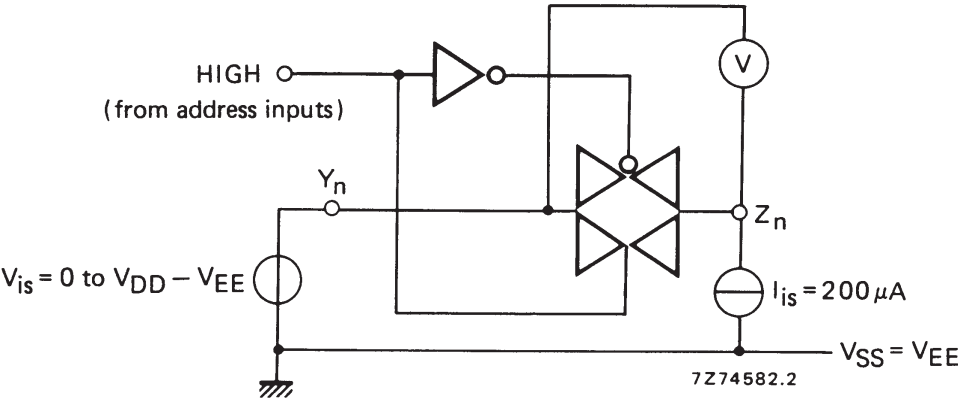


Fig.5 Operating area as a function of the supply voltages.

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$I_{is} = 200 \mu A$
 $V_{SS} = V_{EE} = 0 V$

Fig.7 Typical R_{ON} as a function of input voltage.

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	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	$1\,300 f_i + \sum(f_o C_L) \times V_{DD}^2$ $6\,100 f_i + \sum(f_o C_L) \times V_{DD}^2$ $15\,600 f_i + \sum(f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

AC CHARACTERISTICS $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.	
Propagation delays					
$V_{is} \rightarrow V_{os}$	5		10	20	ns
HIGH to LOW	10	t_{PHL}	5	10	ns
	15		5	10	ns
LOW to HIGH	5	t_{PLH}	10	20	ns
	10		5	10	ns
	15		5	10	ns
$A_n \rightarrow V_{os}$	5		150	305	ns
HIGH to LOW	10	t_{PHL}	65	135	ns
	15		50	100	ns
LOW to HIGH	5	t_{PLH}	150	300	ns
	10		75	150	ns
	15		50	100	ns
Output disable times					
$\bar{E} \rightarrow V_{os}$	5		95	190	ns
HIGH	10	t_{PHZ}	90	180	ns
	15		90	180	ns
LOW	5	t_{PLZ}	100	205	ns
	10		90	180	ns
	15		90	180	ns
Output enable times					
$\bar{E} \rightarrow V_{os}$	5		130	260	ns
HIGH	10	t_{PZH}	55	115	ns
	15		45	85	ns
LOW	5	t_{PZL}	120	240	ns
	10		50	100	ns
	15		35	75	ns

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	V _{DD} V	SYMBOL	TYP.	MAX.	
Distortion, sine-wave response	5 10 15		0,25 0,04 0,04	% % %	note 4
Crosstalk between any two channels	5 10 15		– 1 –	MHz MHz MHz	note 5
Crosstalk; enable or address input to output	5 10 15		– 50 –	mV mV mV	note 6
OFF-state feed-through	5 10 15		– 1 –	MHz MHz MHz	note 7
ON-state frequency response	5 10 15		13 40 70	MHz MHz MHz	note 8

Notes

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{EE}; C_L = 50 pF to V_{EE}; $\bar{E}$ = V_{SS}; V_{is} = V_{DD} (square-wave); see Fig.8.
2. R_L = 10 kΩ; C_L = 50 pF to V_{EE}; $\bar{E}$ = V_{SS}; A_n = V_{DD} (square-wave); V_{is} = V_{DD} and R_L to V_{EE} for t_{PLH}; V_{is} = V_{EE} and R_L to V_{DD} for t_{PHL}; see Fig.8.
3. R_L = 10 kΩ; C_L = 50 pF to V_{EE}; $\bar{E}$ = V_{DD} (square-wave);
V_{is} = V_{DD} and R_L to V_{EE} for t_{PHZ} and t_{PZH};
V_{is} = V_{EE} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig.8.
4. R_L = 10 kΩ; C_L = 15 pF; channel ON; V_{is} = 1/2 V_{DD} (p-p) (sine-wave, symmetrical about 1/2 V_{DD});
f_{is} = 1 kHz; see Fig.9.
5. R_L = 1 kΩ; V_{is} = 1/2 V_{DD} (p-p) (sine-wave, symmetrical about 1/2 V_{DD});

$$20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB; see Fig. 10.}$$

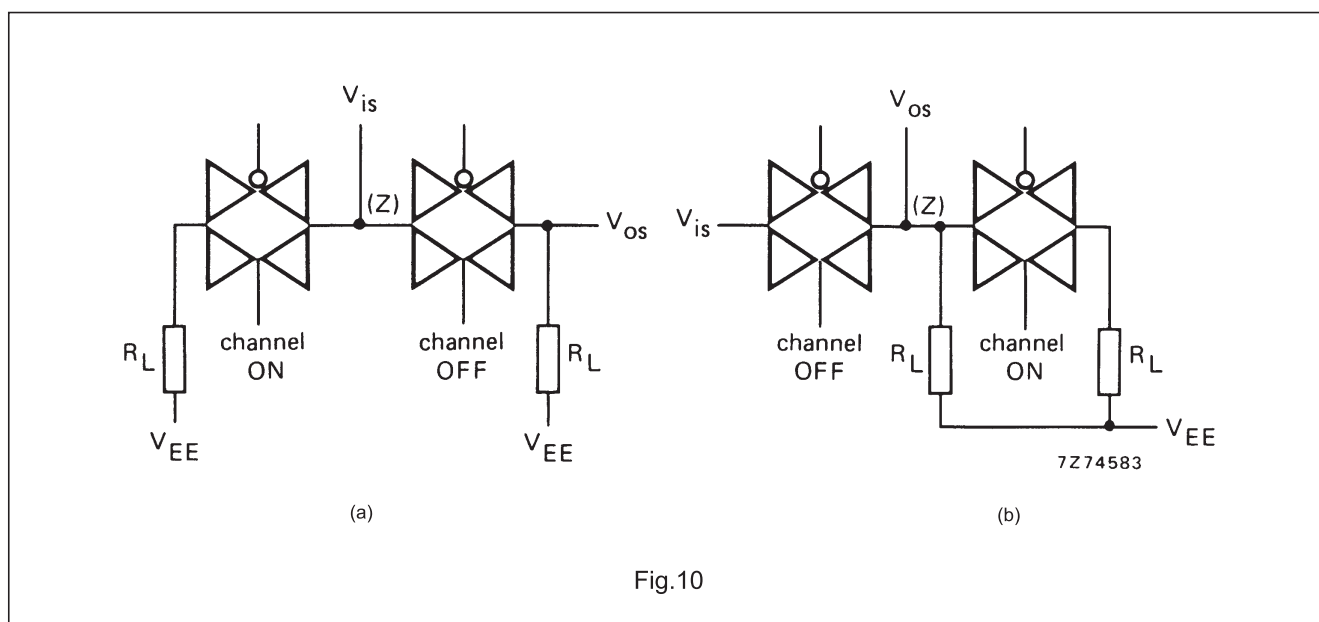
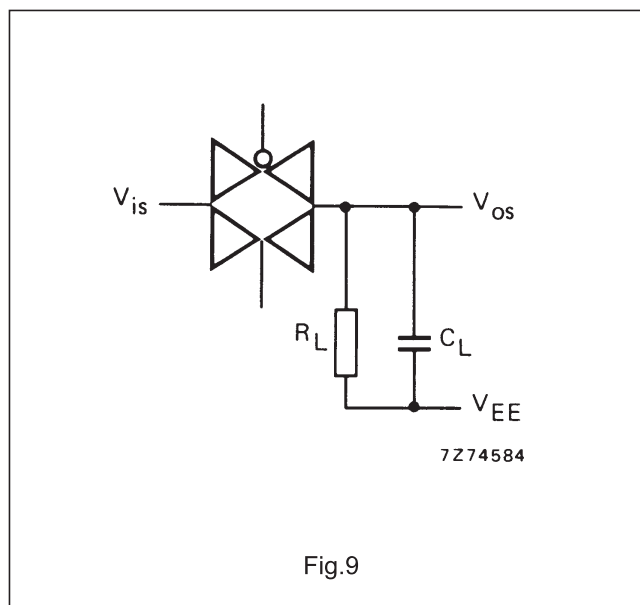
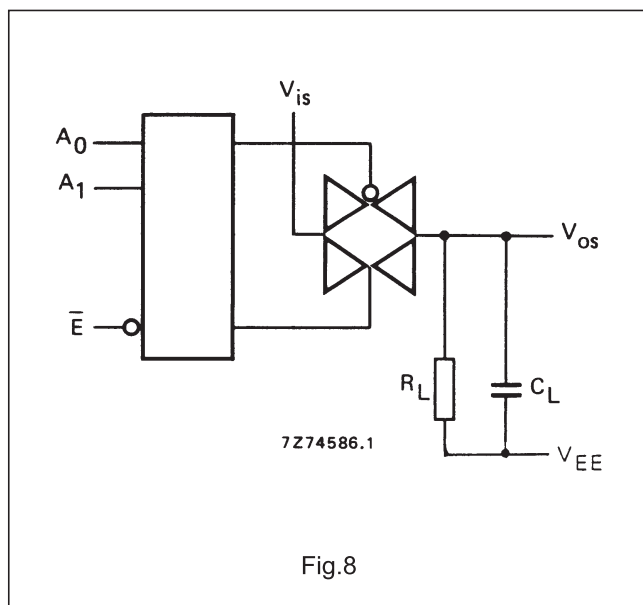
6. R_L = 10 kΩ to V_{EE}; C_L = 15 pF to V_{EE}; $\bar{E}$ or A_n = V_{DD} (square-wave); crosstalk is |V_{os}| (peak value); see Fig.8.
7. R_L = 1 kΩ; C_L = 5 pF; channel OFF; V_{is} = 1/2 V_{DD} (p-p) (sine-wave, symmetrical about 1/2 V_{DD});

$$20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB; see Fig. 9.}$$

8. R_L = 1 kΩ; C_L = 5 pF; channel ON; V_{is} = 1/2 V_{DD} (p-p) (sine-wave, symmetrical about 1/2 V_{DD});

$$20 \log \frac{V_{os}}{V_{is}} = -3 \text{ dB; see Fig. 9.}$$

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APPLICATION INFORMATION

Some examples of applications for the HEF4052B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.