COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

MULTIFUNCTION EXPANDABLE 8-INPUT GATE

- THREE-STATE OUTPUT
- MANY LOGIC FUNCTIONS AVAILABLE IN ONE PACKAGE
- QUIESCENT CURRENT SPECIFIED AT 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4048B** (extended temperature range) and **HCF 4048B** (intermediate temperature range) are monolithic integrated circuit,available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4048B** is an 8-input gate having four control inputs. Three binary control inputs - Ka, Kb, and Kc - provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth control input - Kd- provides the user with a 3-state output. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one **HCC/HCF 4048B**. For example, two **HCC/HCF 4048B**'s can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

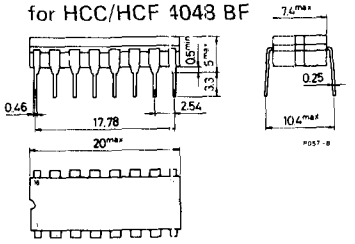
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

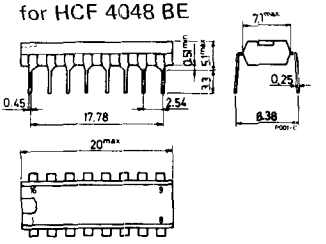
HCC 4048 BD	for dual in-line ceramic package
HCC 4048 BF	for dual in-line ceramic package, frit seal
HCC 4048 BK	for ceramic flat package
HCF 4048 BE	for dual in-line plastic package
HCF 4048 BF	for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

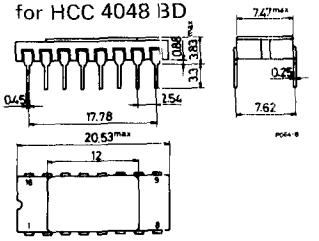
Dual in-line ceramic package
for HCC/HCF 4048 BF



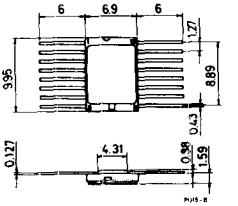
Dual in-line plastic package
for HCF 4048 BE



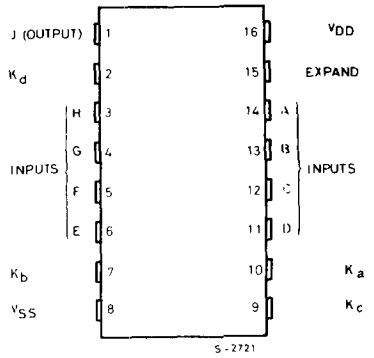
Dual in-line ceramic package
for HCC 4048 BD



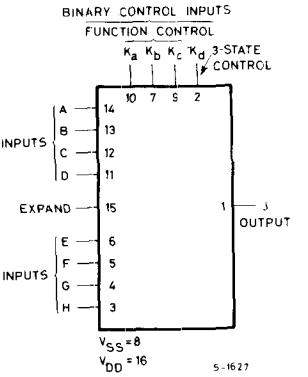
Ceramic flat package
for HCC 4048 BK



CONNECTION DIAGRAM



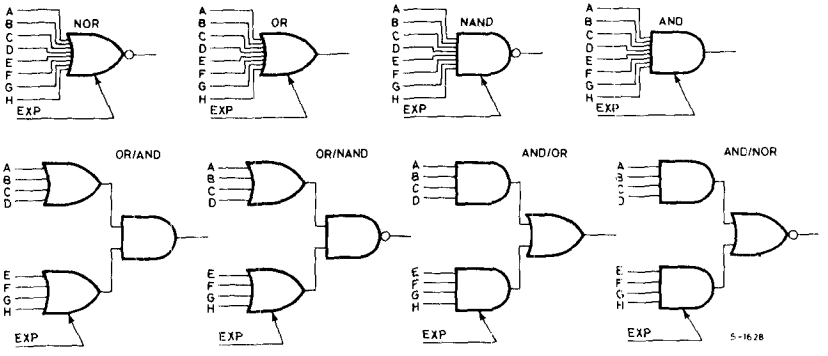
FUNCTIONAL DIAGRAM



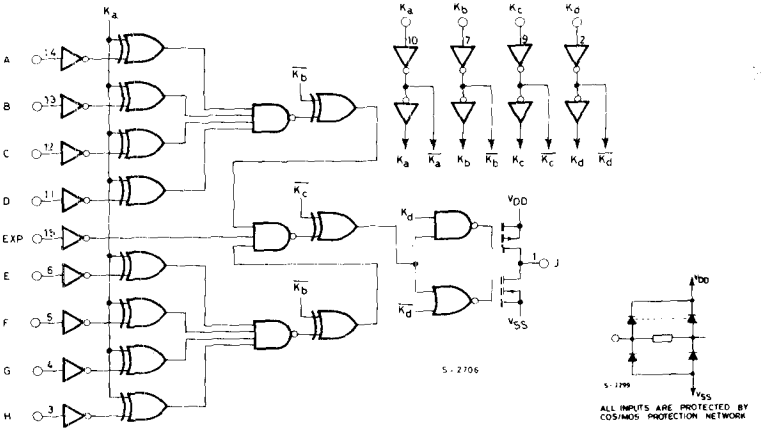
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for HCC types	-55 to 125	°C
	for HCF types	-40 to 85	°C

BASIC LOGIC CONFIGURATIONS



LOGIC DIAGRAM



FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}

$K_d=1$ Normal Inverter Action
$K_d=0$ High Impedance Output

EXPAND Input = 0

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

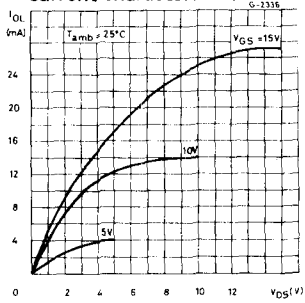
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
I_{OH}	3-state output current		0/18	0/18		18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

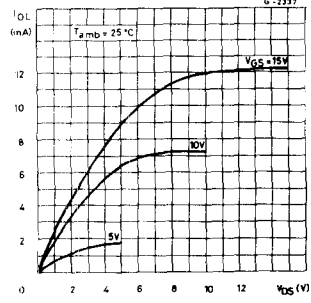
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter*	Test conditions	Values			Unit
	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	5		300		ns
	10		130		
	15		100		
t_{TLH}, t_{THL} Transition time	5		100		ns
	10		50		
	15		40		

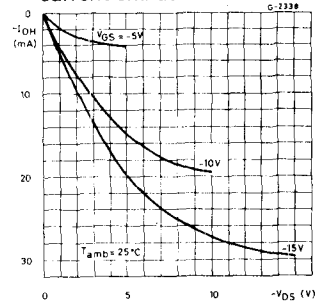
Typical output low (sink) current characteristics



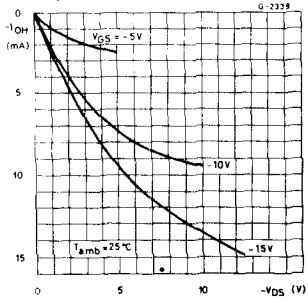
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

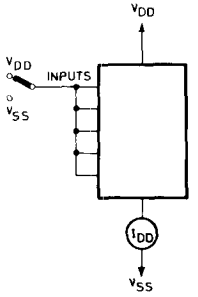


Minimum output high (source) current characteristics

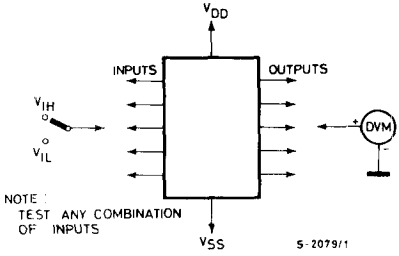


TEST CIRCUITS

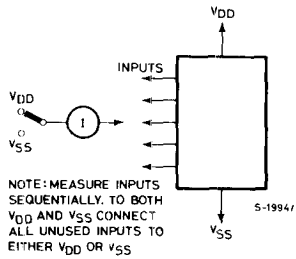
Quiescent device current



Input voltage

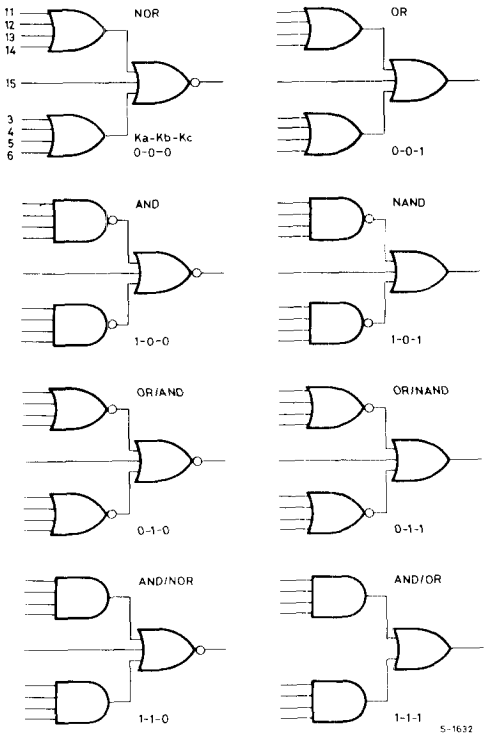


Input current



APPLICATIONS OF EXPAND INPUT

Actual-circuit logic configurations



Expansion logic and truth table

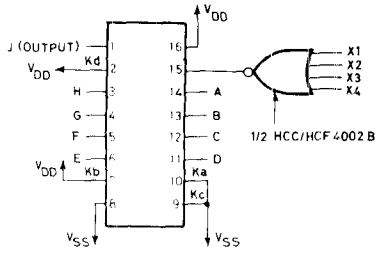
IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J = \overline{(A+B+C+D+E+F+G+H) + (EXP)}$
OR	OR	$J = (A+B+C+D+E+F+G+H) + (EXP)$
AND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
NAND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
OR/AND	NOR	$J = \overline{(A+B+C+D) \cdot (E+F+G+H) \cdot (EXP)}$
OR/NAND	NOR	$J = \overline{(A+B+C+D) \cdot (E+F+G+H) \cdot (EXP)}$
AND/NOR	AND	$J = (ABCD) + (EFGH) + (EXP)$
AND/OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$)

APPLICATIONS (continued)

12-input OR/AND gate



12-INPUT OR/AND GATE
$J=(A+B+C+D)\cdot(E+F+G+H)\cdot(X1+X2+X3+X4)$

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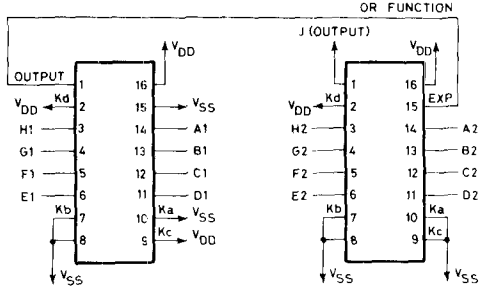
16-input NOR gate



16-INPUT NOR GATE

$J=\overline{A1+B1+C1+D1+E1+F1+G1+H1+A2+B2+C2+D2+E2+F2+G2+H2}$

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