

TC4042BP/BF

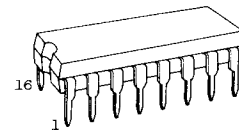
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4042BP/TC4042BF QUAD CLOCKED "D" LATCH

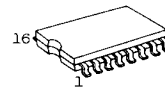
TC4042BP/BF contains four circuits of "D" type latches having common CLOCK input and POLARITY input.

When POLARITY input is placed at "H" level, D input appears as it is at Q output during CLOCK input stays high and D input at the time of falling edge of CLOCK input is retained at Q output. As long as CLOCK input stays low, Q output is not changed even when D input varies.

When POLARITY input is placed "L", D input appears as it is at Q output during CLOCK input stays at "L" level and the latch operation is seen as long as CLOCK input is "H".



DIP16(3D16A-P)

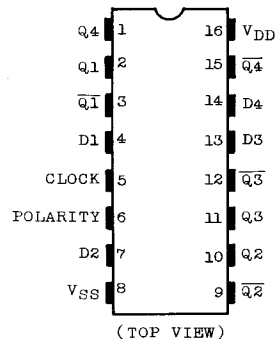


MFP16(F16GC-P)

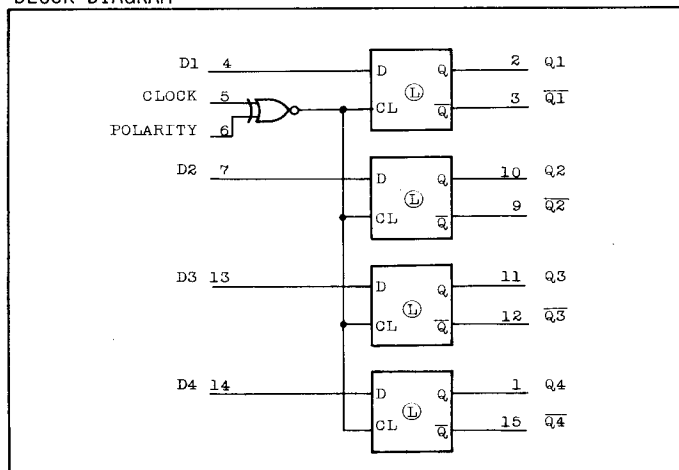
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNITS
DC Supply Voltage	V _{DD}	V _{SS} - 0.5 ~ V _{SS} + 20	V
Input Voltage	V _{IN}	V _{SS} - 0.5 ~ V _{DD} + 0.5	V
Output Voltage	V _{OUT}	V _{SS} - 0.5 ~ V _{DD} + 0.5	V
DC Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T _A	-40 ~ 85	°C
Storage Temperature Range	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C · 10 sec	

PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE

INPUTS		OUTPUTS
CLOCK Δ	POLARITY	Q _n *
H	H	D _n
L	L	D _n
	L	LATCH
	H	LATCH

Δ : Level Change

* : 1 ~ 4

STATIC ELECTRICAL CHARACTERISTICS (Continued)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V _{DD} (V)	-40°C		25°C			85°C		UNITS
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Input Current	"H" Level	I _{IH}	V _{IH} =18V	18	-	0.1	-	10 ⁻⁵	0.1	-	1.0	μA
	"L" Level	I _{IL}	V _{IL} =0V	18	-	-0.1	-	-10 ⁻⁵	-0.1	-	-1.0	
Quiescent Device Current		I _{DD}	V _{IN} =V _{SS} , V _{DD}	5	-	1	-	0.002	1	-	30	
				10	-	2	-	0.004	2	-	60	
				15	-	4	-	0.008	4	-	120	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTICS	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNITS
Output Transisition Time (Low to High)	t _{TLH}		5	-	70	200	ns
			10	-	35	100	
			15	-	30	80	
Output Transition Time (High to Low)	t _{THL}		5	-	70	200	
			10	-	35	100	
			15	-	30	80	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t _{pLH} t _{pHL}		5	-	150	440	
			10	-	70	180	
			15	-	50	120	
Propagation Delay Time (DATA - Q, $\overline{Q}$)	t _{pLH} t _{pHL}		5	-	110	220	
			10	-	55	110	
			15	-	40	80	
Min. Clock Pulse Width	t _w		5	-	55	200	
			10	-	25	100	
			15	-	20	60	
Min. Hold Time (DATA - CLOCK)	t _H		5	-	5	50	
			10	-	3	20	
			15	-	2	20	
Min. Set-up Time (DATA - CLOCK)	t _{SU}		5	-	20	50	
			10	-	10	30	
			15	-	5	25	
Input Capacitance	C _{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

