PRESETTABLE UP/DOWN COUNTER BINARY OR BCD-DECADE

GENERAL DESCRIPTION

The MMC 4029 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.
The MMC 4029 consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, $\overline{\text{CARRY—IN}}$ ($\overline{\text{CLOCK}}$ $\overline{\text{ENABLE}}$), BINARY/DECADE, UP/DOWN, PRESET ENABLE signals. Q1, Q2, Q3, Q4 and a $\overline{\text{CARRY OUT}}$ signal are provided as outputs. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET—ENABLE signal is high, resets the counter to it's zero count. The counter is advanced one count at the positive transition of the clock when the $\overline{\text{CARRY—IN}}$ or PRESET ENABLE signals are high. Advancement is inhibited when the $\overline{\text{CARRY—IN}}$ or PRESET ENABLE signals are high. The $\overline{\text{CARRY—OUT}}$ signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the $\overline{\text{CARRY—IN}}$ signal is low. The $\overline{\text{CARRY—IN}}$ signal in the low state can thus be considered a $\overline{\text{CLOCK}}$ $\overline{\text{ENABLE}}$. The $\overline{\text{CARRY—IN}}$ terminal must be conected to V_{SS} when not in use. Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low.
Multiple packages can be conected in either a parallel-clocking or a ripple-clocking arrangement as shown in cascading counter packages. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

FEATURES

- Medium speed operation—8 MHz (typ.) at C_L = 50 pF and $V_{DD}-V_{SS}$ = 10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "PRESET ENABLE" and individual "JAM" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode

ABSOLUTE MAXIMUM RATINGS

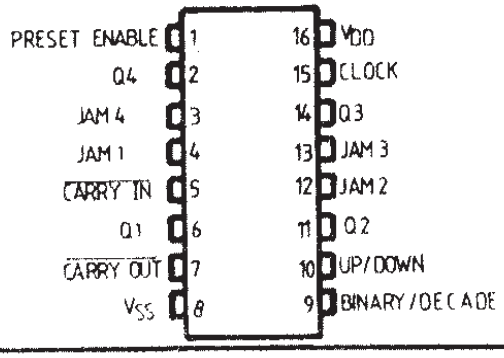
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Imput voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 [5]	±0.1		±1	μA
		E, F types	0/15			15		±0.3		±10 [5]	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices

The Noise Margin for both "1" and "0" level is

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

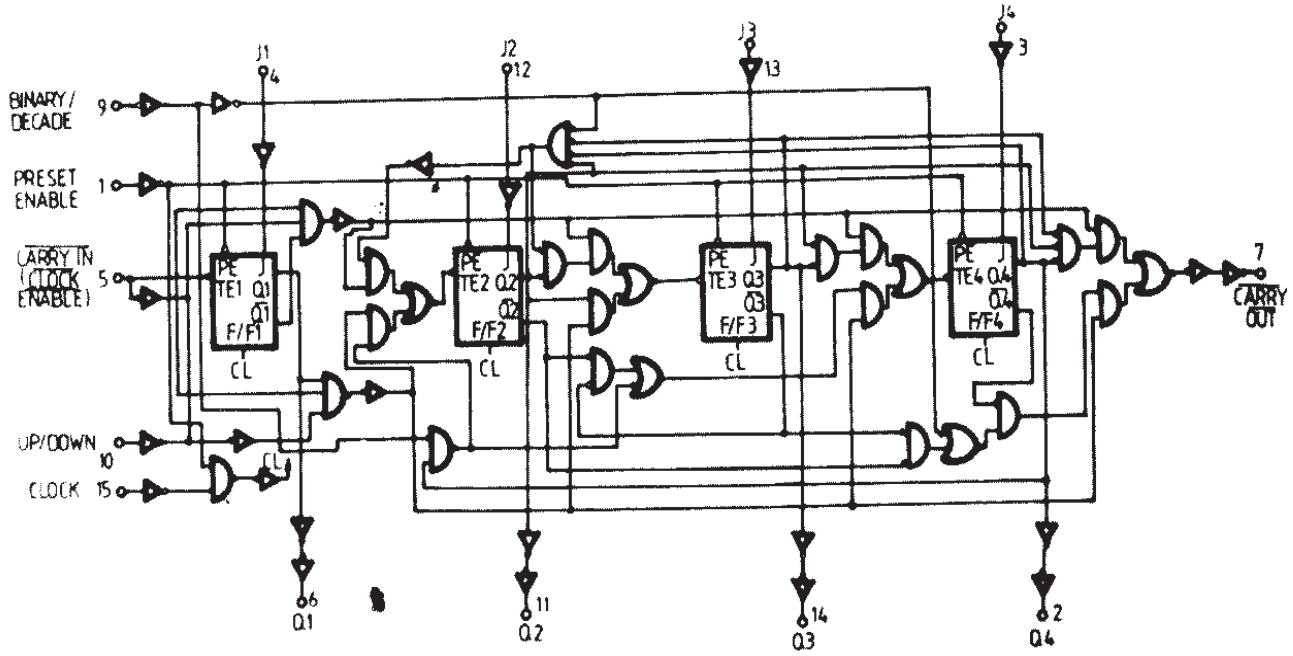
(T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} = 0.3%/°C, all input rise and fall times= 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time (Q outputs)	5		250	500	ns
		10		120	240	
		15		90	180	
t_{PLH}, t_{PHL}	Propagation delay time (Carry Output)	5		280	560	ns
		10		130	260	
		15		95	190	
t_{TLH}, t_{THL}	Transition time (Q outputs, carry output)	5		100	200	ns
		10		50	100	
		15		40	80	
t_W	Minimum clock pulse width	5		90	180	ns
		10		45	90	
		15		30	60	
t_r, t_f*	Clock rise and fall time	5			15	µs
		10			15	
		15			15	
t_{setup}**	Minimum setup time (Carry input)	5		30	60	ns
		10		10	20	
		15		6	12	
t_{setup}	Minimum setup time (B/D or U/D)	5		170	340	ns
		10		70	140	
		15		50	100	
f_{max}	Maximum clock input frequency	5	2	4		MHz
		10	4	8		
		15	5.5	11		
Preset enable						
t_{THL}, t_{TLH}	Propagation delay time (Q outputs)	5		235	470	ns
		10		100	200	
		15		80	160	
t_{PHL}, t_{PLH}	Propagation delay time (Carry Output)	5		320	640	
		10		145	290	
		15		105	210	
t_W	Minimum Preset enable (pulse width)	5		65	130	ns
		10		35	70	
		15		25	50	
t_{rem}**	Minimum preset enable (removal time)	5		100	200	ns
		10		55	110	
		15		40	80	
Carry input						
t_{PHL}, t_{PLH}	Propagation delay time (Carry output)	5		170	340	ns
		10		70	140	
		15		50	100	
t_{setup}***	Minimum setup time (Carry input)	5		25	50	ns
		10		15	30	
		15		12	25	

PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{hold} *** Minimum hold time (Carry input)	5		100	200	ns
	10		35	70	
	15		30	60	

* If more than one unit is cascaded in the parallel clocked application, t_r should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.
** From Up/Down, Binary/Decade, Carry In preset Enable Control Inputs to Clock Edge.
*** From Carry In to Clock Edge.

LOGIC DIAGRAM



TRUTH TABLES

CLOCK	TE	PE	J	Q	$\overline{Q}$
X	X	0	0	0	1
⊓	0	1	X	$\overline{Q}$	Q
X	X	0	1	1	0
⊓	1	1	X	Q	$\overline{Q}$ NC
⊔	X	1	X	Q	$\overline{Q}$ NC

X = don't care

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
$\overline{\text{CARRY IN (CI)}}$ / (CLOCK ENABLE)	1	NO COUNTER ADVANCE AT POSITIVE CLOCK TRANSITION
	0	COUNTER ADVANCE AT POSITIVE CLOCK TRANSITION