Signetics

7495, LS95B
Shift Registers

4-Bit Shift Register
Product Specification

Logic Products

FEATURES
- **Separate negative-edge-triggered shift and parallel load clocks**
- **Common mode control input**
- **Shift right serial input**
- **Synchronous shift or load capabilities**

DESCRIPTION
The '95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has serial Data (D_S) and four parallel Data ($D_0 - D_3$) inputs and four Parallel outputs ($Q_0 - Q_3$). The serial or parallel mode of operation is controlled by a Mode Select input (S) and two Clock inputs ($\overline{CP}_1$ and $\overline{CP}_2$). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected Clock input.

When the Mode Select input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_2$ loads parallel data from the $D_0 - D_3$ inputs into the register. When S is LOW, CP_1 is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_1$ shifts the data from Serial input D_S to Q_0 and transfers the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (shift right). Shift left is accomplished by externally connecting Q_3 to D_2, Q_2 to D_1, Q_1 to D_0, and operating the '95 in the parallel mode (S = HIGH).

In normal operations the Mode Select (S) should change states only when both Clock inputs are LOW. However, changing S from HIGH-to-LOW while $\overline{CP}_2$ is LOW, or changing S from LOW-to-HIGH while $\overline{CP}_1$ is LOW will not cause any changes on the register outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
7495	36MHz	39mA
74LS95B	36MHz	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N7495N, N74LS95BN

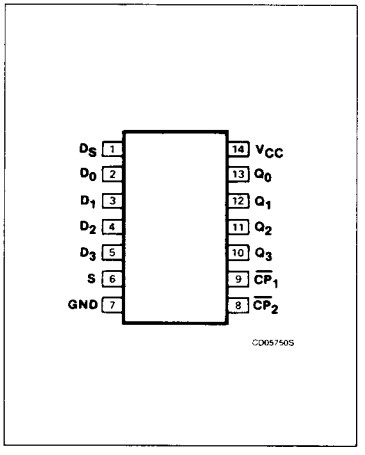
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

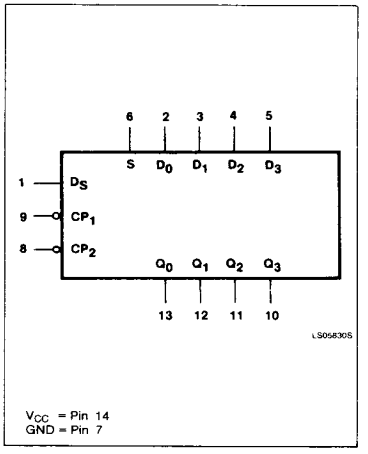
PINS	DESCRIPTION	74	74LS
S	Input	2ul	1LSul
Other	Inputs	1ul	1LSul
Q	Output	10ul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

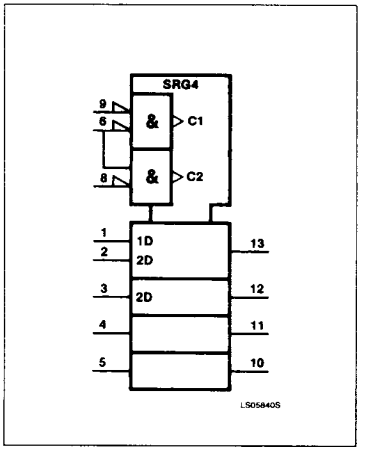
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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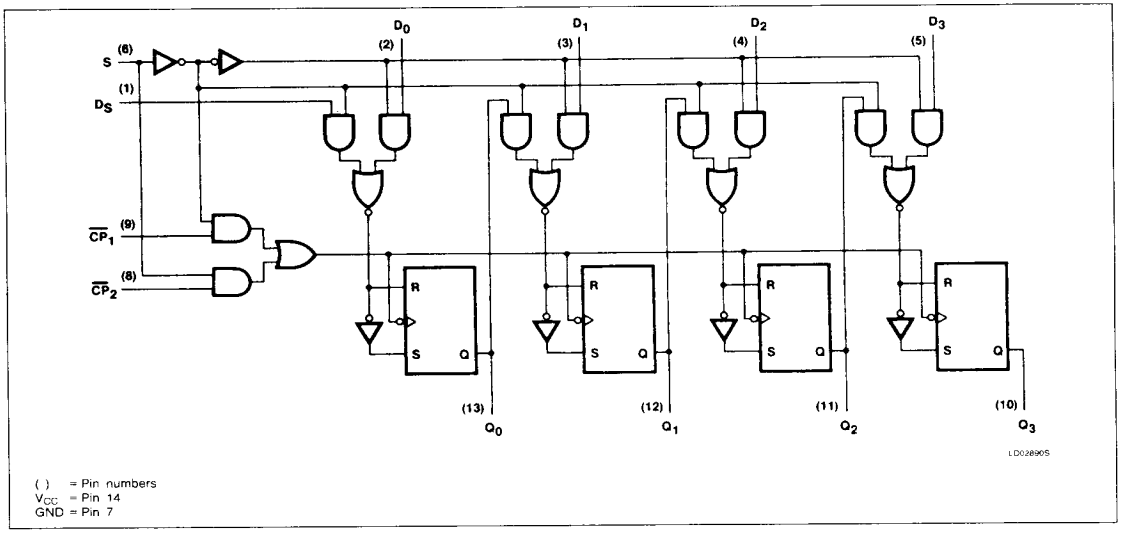
LOGIC DIAGRAM



( ) = Pin numbers
V_{CC} = Pin 14
GND = Pin 7

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FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	CP_1	CP_2	D_S	D_N	Q_0	Q_1	Q_2	Q_3
Parallel load	H	X	↓	X	l	L	L	L	L
	H	X	↓	X	h	H	H	H	H
Shift right	L	↓	X	l	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Mode change	↑	L	X	X	X	no change			
	↑	H	X	X	X	undetermined			
	↓	X	L	X	X	no change			
	↓	X	H	X	X	undetermined			

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition.
q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW clock transition.
X = Don't care.
↓ = HIGH-to-LOW transition of clock or mode select.
↑ = LOW-to-HIGH transition of mode select.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	+0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

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RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18	mA
I_{OH}	HIGH-level output current			−800			−400	μA
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			7495			74LS95B			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX			2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX			0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA (74LS)						0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	S input			80				μA
				Other inputs			40				μA
			V_I = 2.7V	S input						20	μA
				Other inputs						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX V_I = 0.4V		S input			−3.2			−0.4	mA
				Other inputs			−1.6			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−18		−57	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				39	63		13	21	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Serial Data input and all outputs open; Parallel Data inputs grounded; Mode Select input at 4.5V and a momentary 3V, then ground, applied to the Clock inputs.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		MHz
t_{PLH}	Propagation delay Clock to output	Waveform 1		27		27	ns
t_{PHL}				32		32	

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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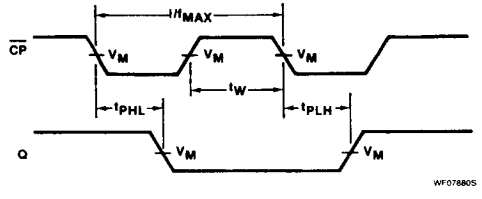
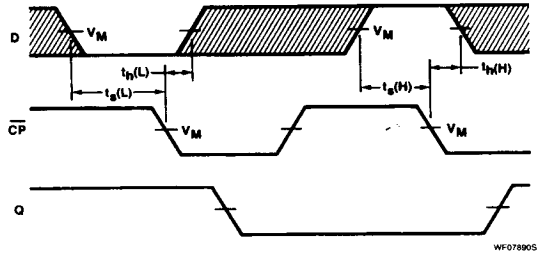
AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
$t_W(H)$	Clock pulse width, HIGH	Waveform 1	20		25		ns
t_s	Set-up time, data to clock	Waveform 2	15		20		ns
t_h	Hold time, data to clock	Waveform 2	0		10		ns
$t_{en}(L)$	Enable time, LOW mode Select to $\overline{CP}_1$	Waveform 3	30		20		ns
$t_{en}(H)$	Enable time, HIGH mode Select to $\overline{CP}_2$	Waveform 3	30		20		ns
$t_{inh}(H)$	Inhibit time, HIGH mode Select to $\overline{CP}_1$ (L → H)	Waveform 3	5		20		ns
$t_{inh}(L)$	Inhibit time, LOW Mode Select to $\overline{CP}_2$ (L → H)	Waveform 3	5		20		ns

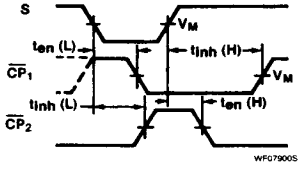
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Data Set-up And Hold Times



For all waveforms, $V_M = 1.5V$ for 74 and 74S; $V_M = 1.3V$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3

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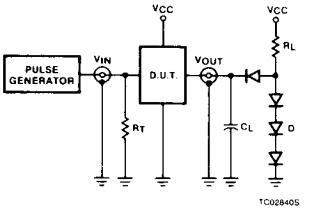
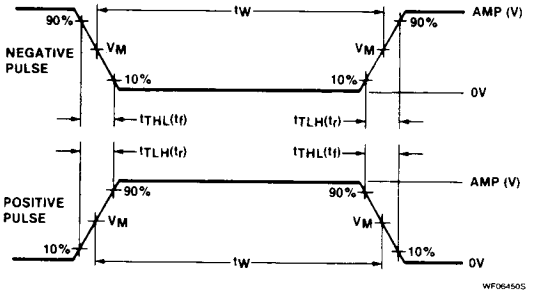
TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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