

DATA SHEET

TDA3842

Multistandard TV IF amplifier and
demodulator with TV signal
identification

Preliminary specification
File under Integrated Circuits, IC02

April 1991

Multistandard TV IF amplifier and demodulator with TV signal identification

TDA3842

FEATURES

- Low supply voltage range, from 5.0 V to 8.0 V
- Low power dissipation, 200 mW at 5 V
- High supply ripple rejection
- Wide IF bandwidth of 80 MHz
- Synchronous demodulator with low differential phase and gain
- Additional video buffer with a wide bandwidth of 10 MHz
- Video off switch
- Peak sync AGC for negative modulation, e.g. B/G
- Peak white AGC for positive modulation, e.g. L
- Adjustable take-over point (TOP); positive AGC slope
- Switching to fast AGC dependent on TV identification
- Alignment free AFC detector with integrated phase shift
- ESD protection
- TV signal identification
- Options: tracking of reference circuit, suitable for MAC-on-cable

GENERAL DESCRIPTION

The TDA3842 is a bipolar integrated circuit for vision IF-signal processing in multistandard TV and VTRs, designed for a supply voltage range from 5.0 V to 8.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5.0	8.8	V
I_P	supply current (pin 15)	$V_P = 5.0$ V	–	42	–	mA
$V_{1-20(rms)}$	IF input signal for nominal video output voltage at pin 14 (RMS value)	$f = 38.9$ MHz	–	70	–	μ V
	minimum IF input signal for TV signal identification at pin 6 (RMS value)	maximum G_V	–	20	40	μ V
V_O	video output signal (pin 12)	buffered	–	2.0	–	V
G_V	IF voltage gain control range		–	66	–	dB
S/N	signal-to-noise ratio	$V_{1-20} = 10$ mV	55	60	–	dB
V_8	AFC output voltage swing		–	4.0	–	V
S_{AFC}	AFC steepness (pin 8)		–	2	–	μ A/kHz
RR	supply voltage ripple rejection (pin 12)		30	35	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3842	20	DIL	plastic	SOT146 ⁽¹⁾
TDA3842T	20	mini-pack	plastic	SO20L; SOT163A ⁽²⁾

Notes

1. SOT146-1; 1997 January 08.
2. SOT163-1; 1997 January 08

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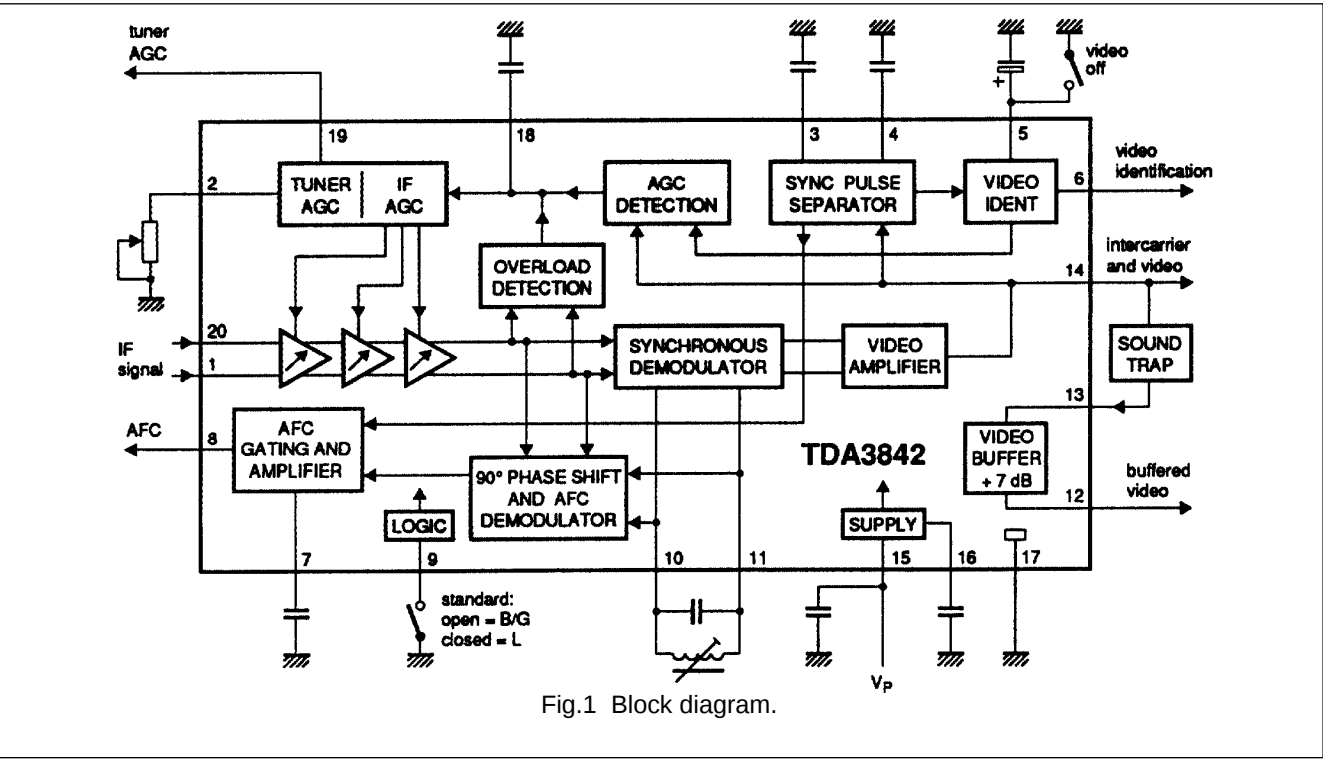


Fig.1 Block diagram.

PIN CONFIGURATION

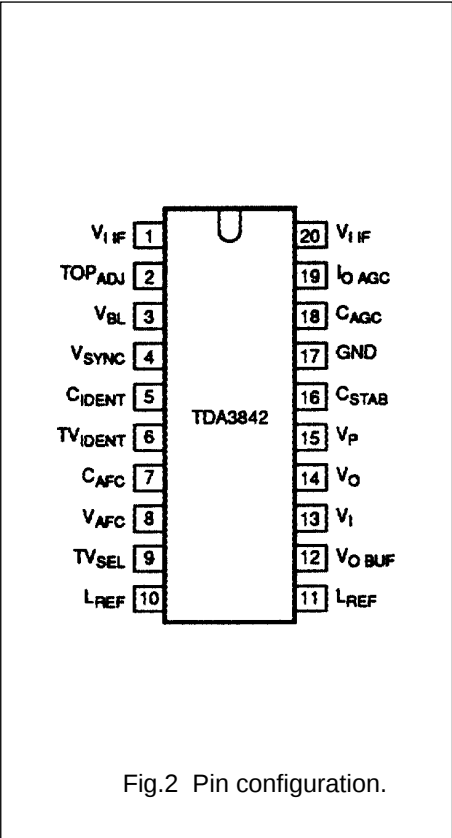


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V _I IF	1	IF input (balanced)
TOP _{ADJ}	2	tuner AGC take-over point adjustment
V _{BL}	3	black level voltage
V _{SYNC}	4	sync pulse amplitude voltage
C _{IDENT}	5	identification capacitor
TV _{IDENT}	6	video identification output
C _{AFC}	7	AFC capacitor
V _{AFC}	8	AFC output signal
TV _{SEL}	9	video standard selection switch
L _{REF}	10	LC reference tuned circuit
L _{REF}	11	LC reference tuned circuit
V _O BUF	12	buffered video output signal
V _I	13	video input signal for buffer
V _O	14	video output signal with intercarrier signal
V _P	15	supply voltage
C _{STAB}	16	supply voltage stabilization
GND	17	ground
C _{AGC}	18	AGC capacitor
I _O AGC	19	tuner AGC output signal
V _I IF	20	IF input (balanced)

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FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. 3-stage gain controlled IF amplifier
2. Overload detector
3. Reference amplifier
4. Carrier signal reference limiter
5. Video demodulator
6. Video amplifier
7. Video buffer amplifier
8. AGC detector
9. IF and tuner AGC (with adjustable TOP)
10. Sync pulse separator
11. Video identification
12. 90° phase shift and AFC demodulator
13. AFC gating, AFC amplifier and AFC switch
14. Voltage stabilizer
15. Standard switch

1. 3-stage gain controlled IF amplifier (pins 1 and 20)

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Gain control is achieved by current divider stages. The emitter feedback resistors are optimized for low noise and signal handling capability.

2. Overload detector

The overload detector is fed from the output of the third IF amplifier. As soon as the IF voltage exceeds the overload threshold in the detector, its output current reduces the IF amplification by discharging the AGC capacitor.

3. Reference amplifier

For passive video carrier regeneration an integrated differential amplifier with resistive load allows

capacitive coupling of the resonant circuit for notch and tracking functions.

4. Carrier signal reference limiter

A limiter stage after the reference amplifier eliminates amplitude modulation. Its output is fed to the video demodulator.

5. Video demodulator

The video demodulator receives both the limited reference carrier signal and the IF signal. The video signal polarity is switched according to the TV standard selected. The video signal can also be switched off.

6. Video amplifier

The video amplifier is an operational amplifier with internal feedback and wide bandwidth. The DC level is shifted according to the TV standard to provide the same sync level for positive and negative IF modulation.

7. Video buffer amplifier

The video buffer amplifier is an operational amplifier with internal feedback, wide bandwidth and frequency compensation; gain and input impedance are adapted to operate with a ceramic sound trap. The load for the sound trap is an integrated resistive divider.

8. AGC detector

With negative modulation (B/G) a peak sync AGC detector generates a fast current pulse to discharge the AGC capacitor (gain reduction). This minimizes the video signal distortion. *Positive modulation (L)* uses a peak white AGC detector.

To filter out the sound carrier the video signal is fed through low pass filters. After the low pass filters the video signal with attenuated sound carrier, is fed to the AGC detector.

The charging current of the AGC capacitor is optimized for minimum distortion of the video signal. With positive modulation the charging current is very low and consequently the AGC time constant is large. When the video identification circuit does not detect a video signal, the charging current is increased.

9. IF and tuner AGC

The voltage on the AGC capacitor is used to control the gain of the three IF amplifier stages and to supply the tuner AGC current (open-collector). The tuner AGC TOP potentiometer at pin 2 adjusts the IF signal level from the tuner. To stabilize the IF output voltage of the tuner, IF slip (= variation of IF gain over the total tuner range) is kept at a minimum.

10. Sync pulse separator

The sync pulse separator supplies two internally-used pulses using the bandwidth limited video signal. These are the composite sync for the AFC detector and the vertical sync for the video identification output. The bandwidth is limited to reduce the noise and increase the ident sensitivity.

11. Video identification

An analog integrator monitors the duty cycle of the vertical sync pulses to identify the video signal. The integrator output is fed to a window comparator which has an open collector output stage to provide the video ident signal. The complete circuit operates in combination with the sync separator and is optimized for high sensitivity.

12. 90° phase shift and AFC demodulator

The AFC demodulator needs a 90° phase-shifted carrier. The output of the carrier signal reference limiter is

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fed to an active 90° phase-shift circuit. The 90° (lead) phase-shifted carrier and the IF signal are fed to the AFC demodulator. The demodulated signal is fed to the AFC gating stage.

13. AFC gating, AFC amplifier and AFC switch

With negative modulated video IF signals the output of the AFC detector is gated by composite sync pulses to prevent video modulation on the AFC

output. The gated signal is integrated by an AFC capacitor. The AFC amplifier converts the capacitor voltage to an AFC current (open collector sink/source output). At positive modulation the AFC operates continuously.

AFC function can be externally switched off for test purposes. For high-performance signal handling the AFC signal can be used to track the resonant circuit as shown in Fig.11.

14. Voltage stabilizer

An integrated bandgap voltage stabilizer generates an internal supply voltage of 4 V. A decoupling capacitor reduces noise and supply voltage ripple.

15. Standard switch

The operating mode of the AGC detector and video IF demodulator for positive and negative IF modulation is selected by the logic level on pin 9.

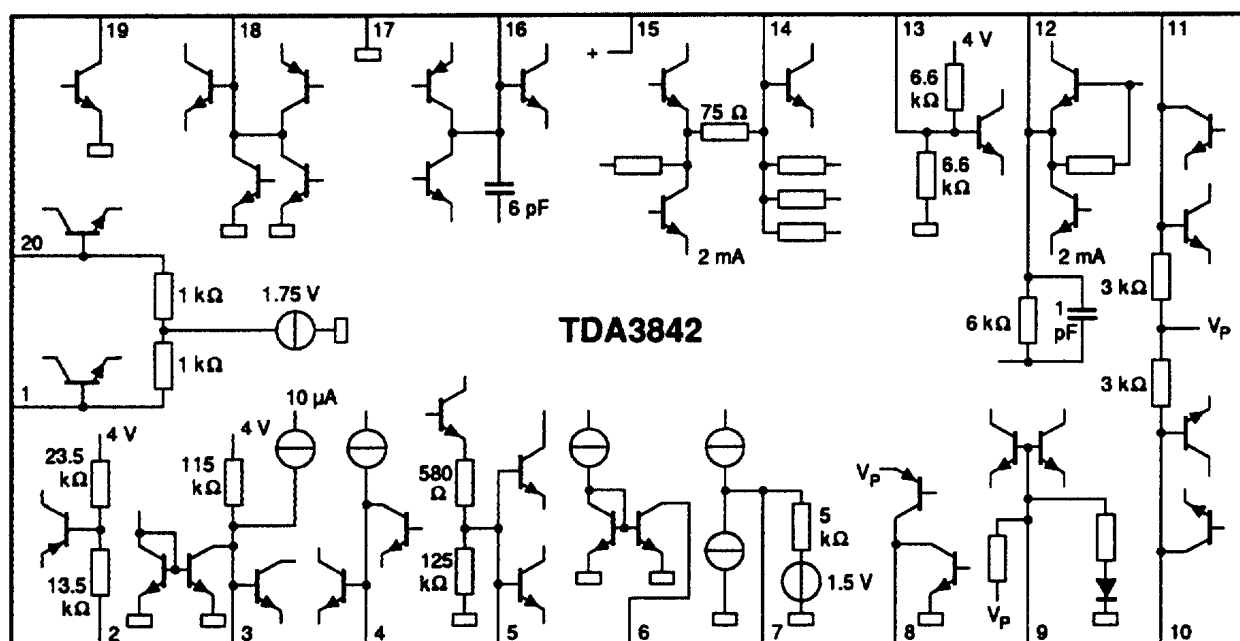


Fig.3 Internal circuits.

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage at pin 15:	SOT146	8.8	V
		SOT163A	6.0	V
V_{19}	tuner AGC voltage	–	13.2	V
V_8	permissible voltage at AFC output	–	V_P	V
I_{15}	supply current	–	55	mA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
V_{ESD}	ESD sensitivity	–	± 300	V

CHARACTERISTICS

$V_P = 5\text{ V}$ and $T_{amb} = 25\text{ °C}$; $f_{VC} = 38.9\text{ MHz}$; all voltages are measured to GND (pin 17); measured in test circuit of Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _P	supply voltage range (pin 15)	DIL-package	4.75	5.0	8.8	V
		SO-package	4.75	5.0	6.0	V
I _P	supply current (pin 15)	V _P = 5.0 V	–	42	–	mA
RR	ripple rejection (pin 12)		30	35	–	dB
IF amplifier						
B	bandwidth	–3 dB	–	80	–	MHz
R _I	input resistance (pins 1 and 20)		–	2	–	kΩ
C _I	input capacitance (pins 1 and 20)		–	1.5	–	pF
V _{1-20(rms)}	IF input signal (RMS value)	video output –1 dB	–	70	–	μV
	maximum IF input signal	minimum G _V ; note 1	100	–	–	mV
G _V	gain control range		63	66	–	dB
IF AGC: negative modulation						
I ₁₈	leakage current AGC capacitor		–	–	1	μA
	charging current AGC capacitor	with video identification	–	13	–	μA
	charging current AGC capacitor	without video identification	–	35	–	μA
I _{18M}	discharging peak current capacitor		–	2	–	mA
t ₁	response time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	150	–	ms
IF AGC: standard L (note 2)						
I ₁₈	leakage current AGC capacitor		–	–	20	nA
	charging current AGC capacitor	with video identification	–	280	–	nA
		without video identification	–	22	–	μA
I _{18M}	discharging peak current capacitor		–	2	–	mA
t ₂	response time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	300	–	ms

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner AGC (note 3)						
V _{1-20(rms)}	lower IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R ₂ = 22 kΩ	–	–	1	mV
	upper IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R ₂ = 0 Ω	50	–	–	mV
	TOP variation	60 K temperature range	–	2	3	dB
I ₁₉	tuner AGC output current	V ₁₉ = 0.5 V	1	2	–	mA
Sync demodulator and video amplifier (note 4)						
V ₁₄	composite video output signal		0.9	1.0	1.1	V
	sync level voltage	standard B/G	–	1.5	–	V
	zero carrier level voltage	negative modulation	–	2.6	–	V
		positive modulation	–	1.47	–	V
I ₁₄	output current	DC and AC	–	–	± 1.0	mA
R ₁₄	output resistance		–	75	–	Ω
B	video bandwidth at –1 dB (pin 14)	C _{load} ≤ 20 pF	7	8	–	MHz
V ₁₄	upper video clipping level		–	3.6	–	V
	lower video clipping level		–	0.3	–	V
Buffered video output signal (see Fig.6)						
G	gain of video buffer		6.5	7.0	–	dB
V ₁₂	sync level clamping voltage		–	1.35	–	V
	upper video clipping level		–	4.25	–	V
	lower video clipping level		–	0.3	–	V
I ₁₂	output current	DC and AC	–	–	± 1.0	mA
R ₁₂	output resistance		–	–	10	Ω
B	video bandwidth at –1 dB (pin 12)	C _{load} ≤ 20 pF	–	10	–	MHz
R _I	input resistance (pin 13)		–	3.3	–	kΩ
C _I	input capacitance (pin 13)		–	2	–	pF
Overall video performance (see Fig.6)						
V _o	video output signal (pin 12)	negative modulation	–	2	–	V
		positive modulation; note 4	–	2	–	V
B	video bandwidth at –2 dB (pin 12)	C _{load} ≤ 20 F	7	8	–	MHz
S/N	signal to noise ratio (see Fig.7)	V ₁₋₂₀ = 10 mV; note 5	55	60	–	dB
α ₁	intermodulation for blue (note 6)	f = 1.1 MHz	56	58	–	dB
		f = 3.3 MHz	62	–	–	dB
α ₂	intermodulation for yellow (note 6)	f = 1.1 MHz	53	56	–	dB
		f = 3.3 MHz	60	–	–	dB
α ₃	signal harmonic suppression		–	26	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_5	video switch off voltage	note 7	—	—	1	V
α_4	attenuation of video signal (pin 14)	video signal switched off	50	60	—	dB
ΔG	differential gain	EBU test line 330	—	2	—	%
$\Delta \Phi$	differential phase	EBU test line 330	—	2	—	deg
$\Delta V/V$	variation of video output signal (pin 14)	gain control 50 dB; $V_{1-20(rms)} = 0.3$ to 100 mV	—	—	0.5	dB
V_{res1}	residual vision carrier (pin 12)		—	1	—	mV
V_{res2}	residual second harmonic of the vision carrier (pin 12)		—	1	—	mV
Video identification						
$V_{1-20(rms)}$	minimum IF input signal for TV identification at pin 14 (RMS value)	maximum G_v	—	20	40	μV
V_6	video identification voltage (signal unidentified)	$V_{1-20(rms)} = < 40 \mu V$ $I_6 = 0.5$ mA	—	—	0.4	V
	video identification voltage (signal identified)	$V_{1-20(rms)} = \geq 40 \mu V$ $I_6 = -1 \mu A$	4.5	—	—	V
T_{sync}/T_{field}	vertical pulse duty cycle		4.5	8	16	$\times 10^{-3}$
C/N	carrier-to-noise ratio (pin 1 and pin 20)	note 8	—	8	—	dB
I_5	allowed leakage current		—	—	3	μA
α_5	sync pulse suppression for correct TV signal identification		—	—	70	%
t_d	delay time of mute output signal		—	100	150	ms
AFC (see Fig.9 and Fig.10); note 9						
I_8	AFC source current output		0.16	0.19	0.22	mA
	AFC sink current output		0.16	0.19	0.22	mA
V_8	upper output voltage		4.3	—	4.7	V
	lower output voltage		0.3	—	0.7	V
S	control steepness	$Q_B = 40$; $V_{1-20(rms)} = 10$ mV	—	2	—	$\mu A/kHz$
I_7	leakage current at AFC gating		—	—	± 1	μA
Standard switch						
V_9	voltage for negative modulation	standard switch open	2.5	n.c.	V_P	V
	voltage for positive modulation (L)	standard switch closed	0	—	0.8	V

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Notes to the characteristics

1. The video signal is still gain-controlled, $V_{14(p-p)} = 1\text{ V}$, but intermodulation figures are degraded.
2. In multi-standard applications the capacitor at pin 18 must be a low-leakage (foil) type.
3. The starting point of tuner AGC can be adjusted by the resistor at pin 2. Fig.5 shows the AGC characteristic.
4. IF input signals are RMS values measured at TOP sync (standard B/G) and with a vision carrier of 38.9 MHz (see Fig.4). The IF input signal is fed from $50\ \Omega$ via a 1:1 transformer, DSB, to pins 1 and 20. With a $10\text{ mV}_{\text{RMS}}$ IF input signal, the residual vision carrier is: = 10% for white (standard B/G), = 3% for sync (standard L).
5. In the test circuit of Fig.4, measured and weighted according to CCIR Recommendation 567:

$$S/N = \frac{V_{14 \text{ (black to white)}}}{V_{14 \text{ noise (RMS, black)}}$$

6. Intermodulation figures are defined as follows: $\alpha_1 = 20 \times \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$

$$\text{and } \alpha_2 = 20 \times \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$$

7. When $V_5 < 1\text{ V}$ (short-circuited identification capacitor at pin 5) the video output signal at pin 14 is switched off. V_{14} shifts to "zero carrier level" ("ultra white" (2.6V) for negative modulation or "top sync" (1.5 V) for positive modulation). During normal operation the capacitor at pin 5 should not be loaded ($|I_5| \leq 3\ \mu\text{A}$).
8. The C/N at the IF input (pins 1 and 20) for TV identification is defined as the RMS sync level of the vision IF signal input, relative to the RMS value of a superimposed white noise signal, with a bandwidth limited to 5 MHz.
9. The values for the AFC measurements depend on the Q_B of the reference circuit at pins 10 and 11. The internal phase shift is matched to a vision carrier of 38.9 MHz. The AFC function can be switched off for test purposes when pin 7 is connected to ground ($V_7 = 0\text{ V}$).

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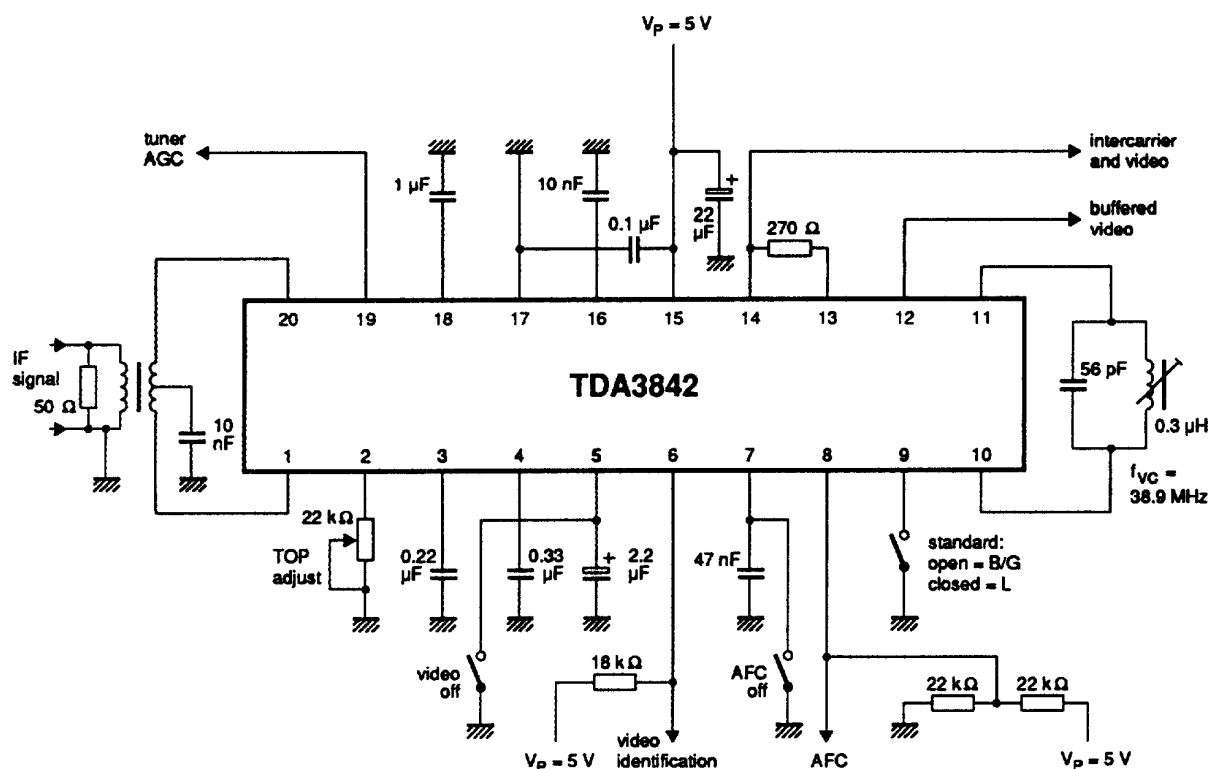


Fig.4 Test circuit.

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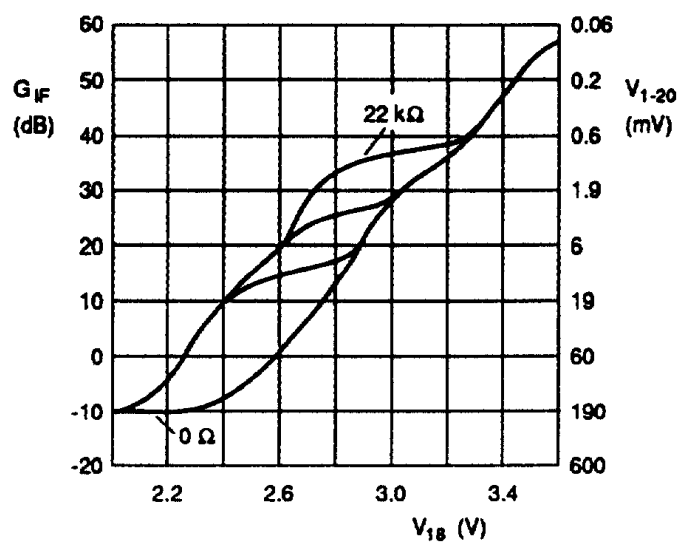


Fig.5 AGC characteristics with different values of R2.

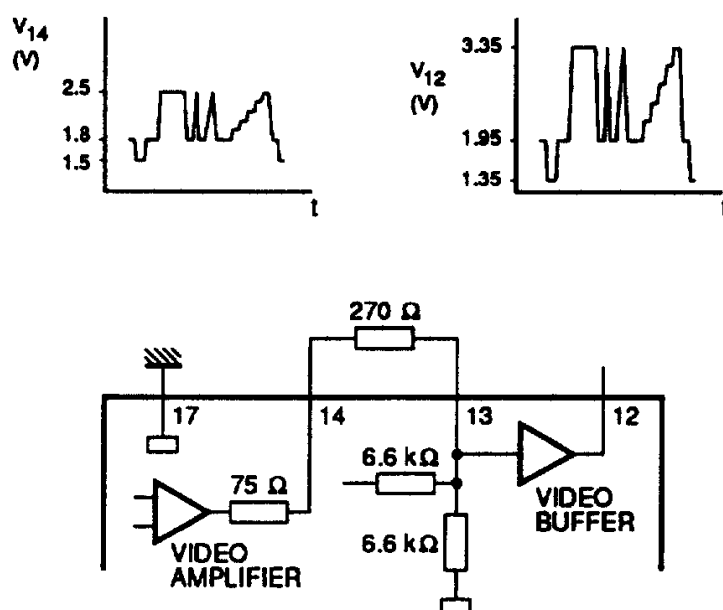


Fig.6 Video waveforms at intercarrier (pin 14) and buffered video (pin 12) outputs.

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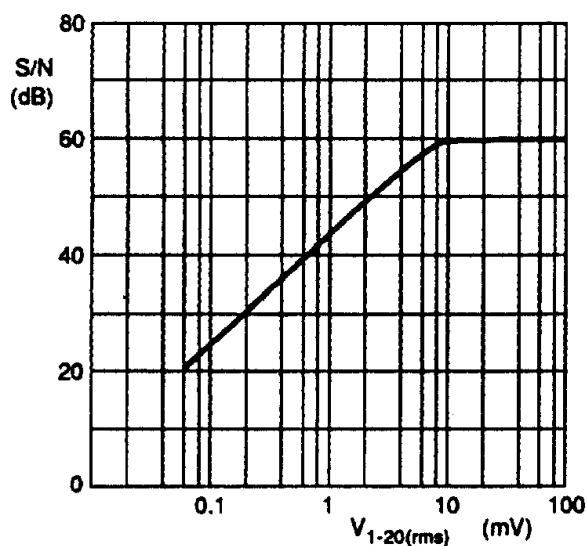
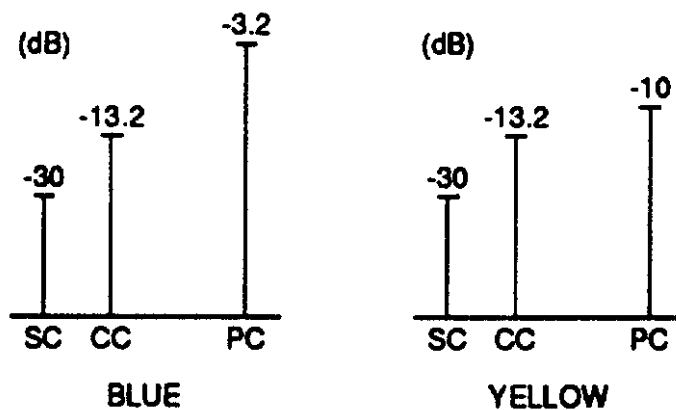


Fig.7 Signal-to-noise ratio as a function of IF input voltage (RMS value) at pins 1 and 20.



SC = sound carrier level; with respect to TOP sync level
 CC = chrominance carrier level; with respect to TOP sync level
 PC = picture carrier level; with respect to TOP sync level

Sound trap attenuation: 17 dB

Fig.8 Input conditions for intermodulation measurements.

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APPLICATION INFORMATION

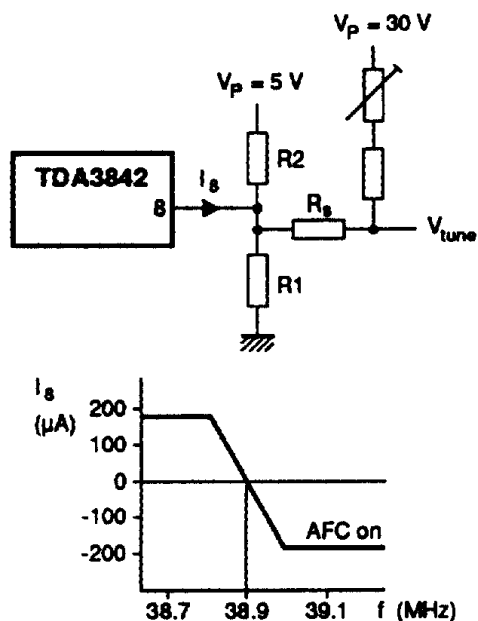
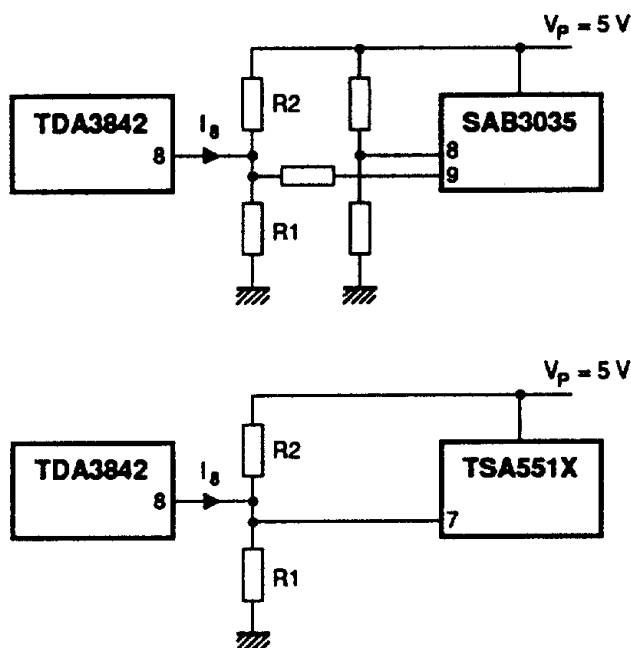


Fig.9 AFC interfacing for analog tuning systems and AFC characteristic.

Fig.10 AFC interfacing for μP controlled systems.

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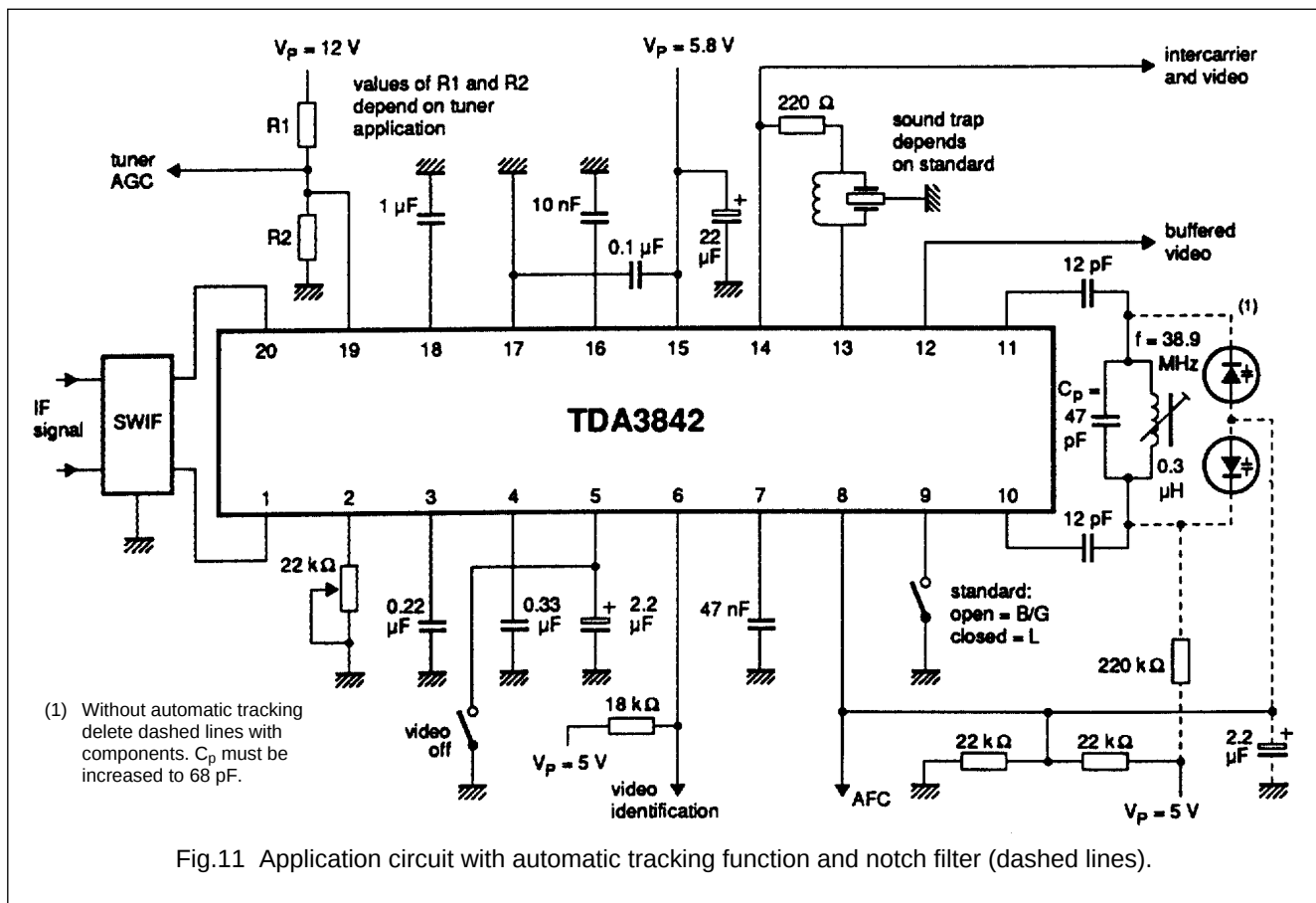


Fig.11 Application circuit with automatic tracking function and notch filter (dashed lines).

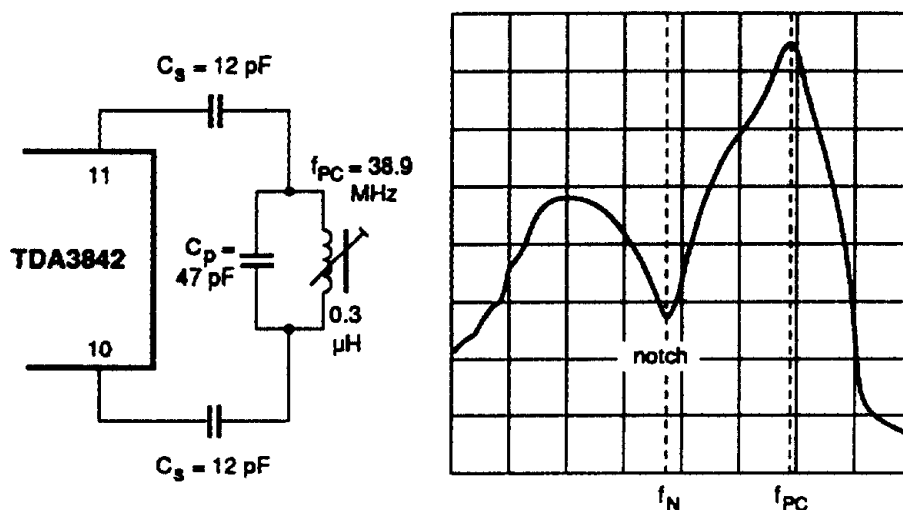


Fig.12 Reference circuit with notch filter for improved pulse response and better signal linearity.

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Note to Fig.12

Recommended for reception of data signals e.g. in Teletext and D2-MAC. Values in combination with SAW filter OFW G 1956 (Siemens). Curve shows combined frequency response of SAW filter and reference circuit.

For different standards C_s and C_p are calculated as follows: $C_s = 2 C_p \left\{ \frac{f_{PC}^2}{f_N^2} - 1 \right\}$

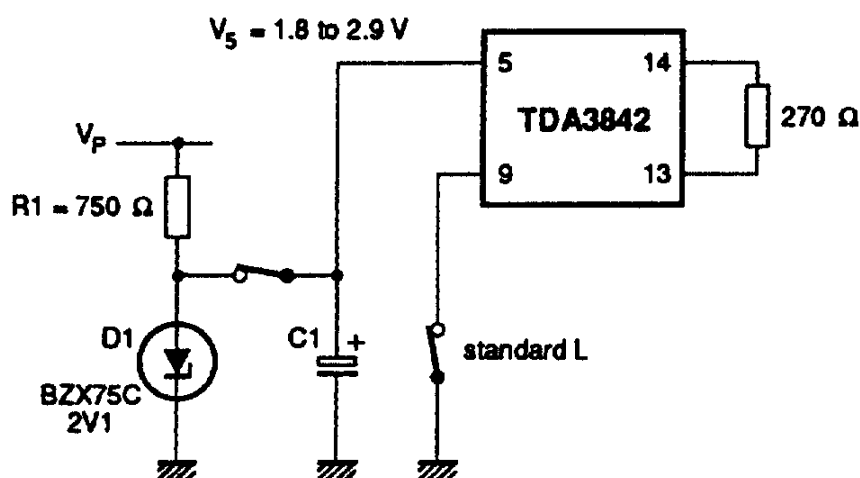


Fig.13 Modification of Fig.11 for MAC/D2-MAC application.

Note to Fig.13

When the TDA3842 is used in a MAC/D2-MAC receiver the voltage at pin 5 must be stabilized between 1.8 and 2.9 V by zener diode D1 and resistor R1. Standard switch at pin 9 must be in position 'standard L' to activate the peak-related slow AGC mode.

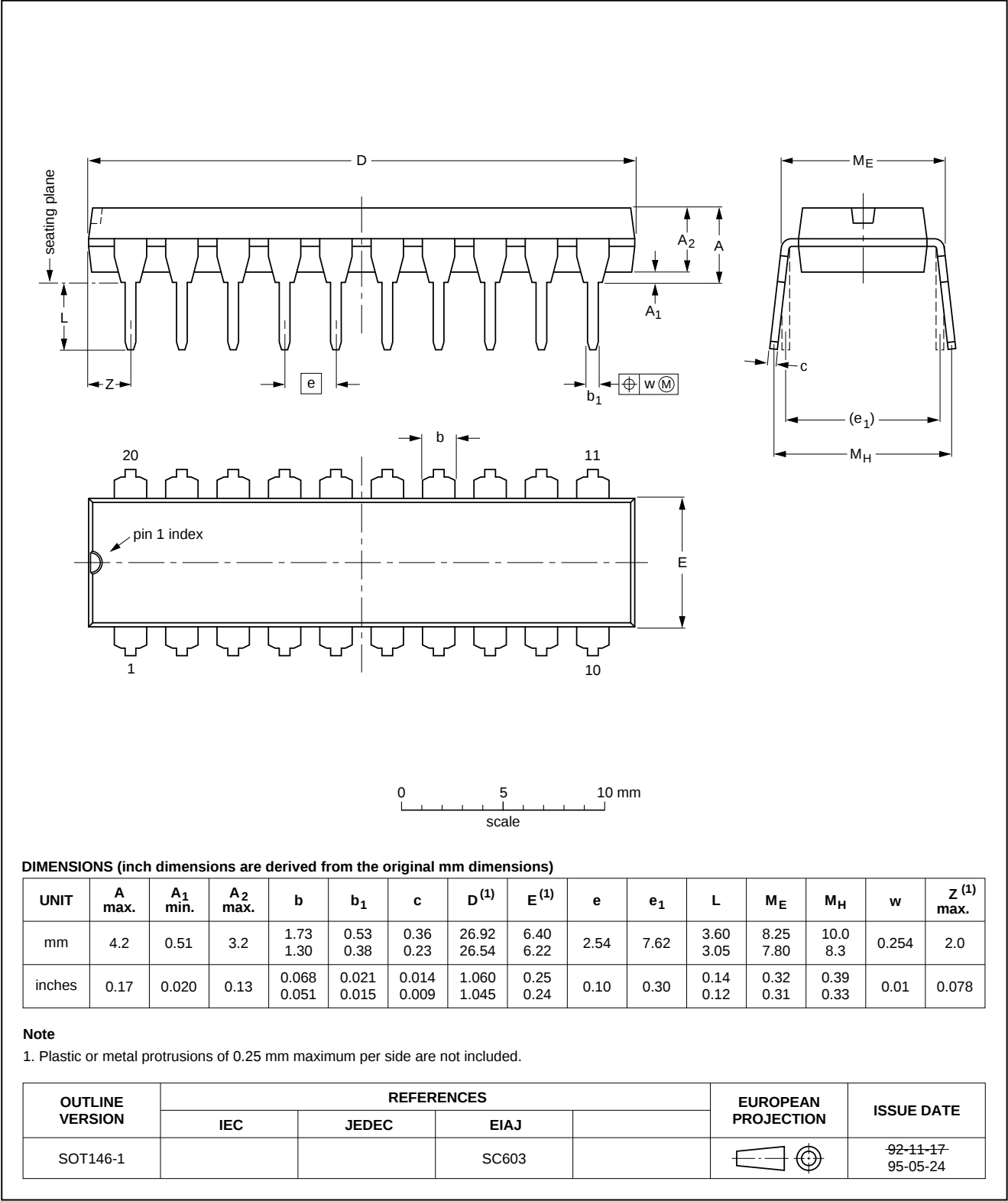
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PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

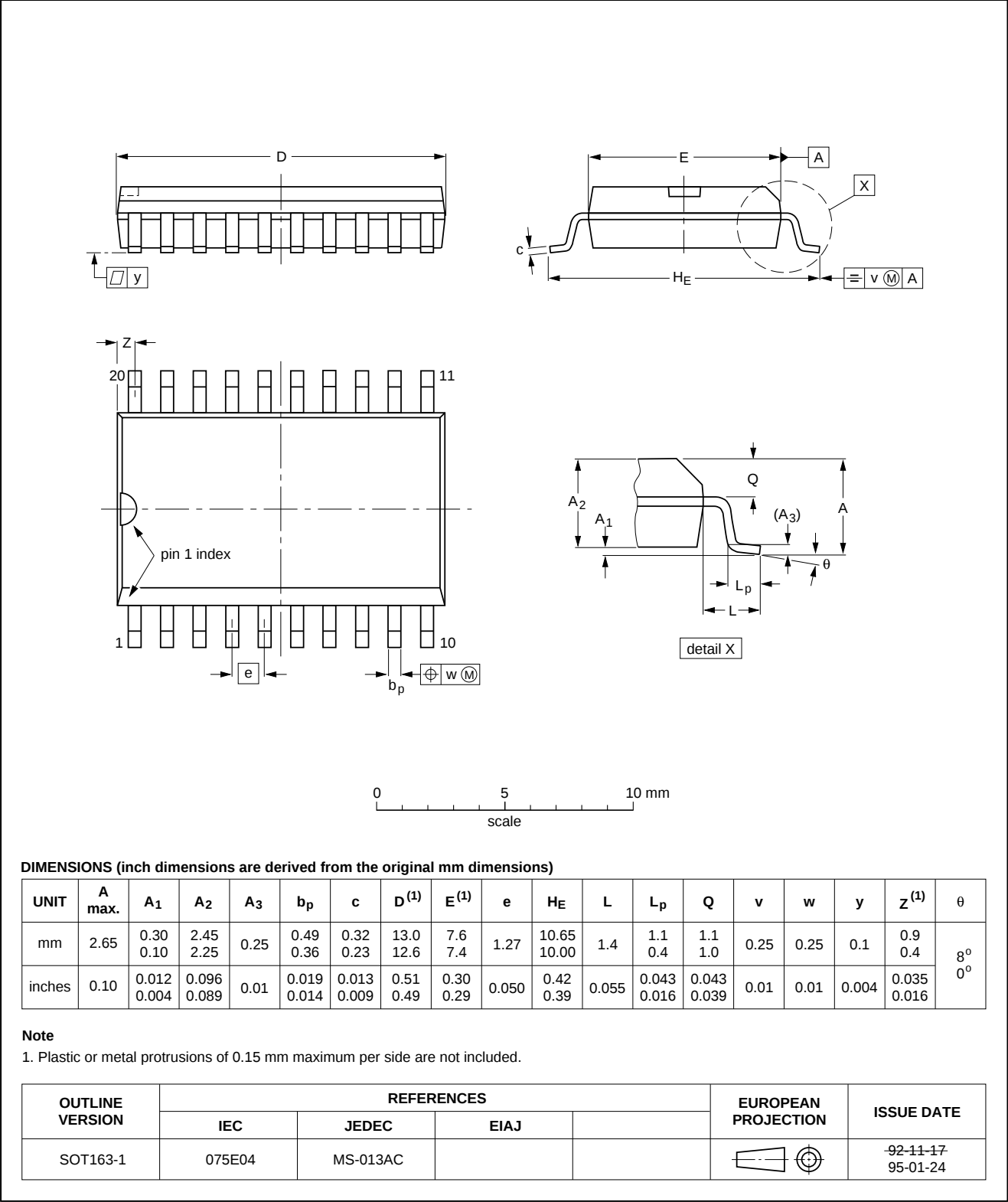


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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.