LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TDA2560 is a monolithic integrated circuit for use in decoding systems of colour television receivers. The circuit consists of a luminance and chrominance amplifier. The luminance amplifier has a low input impedance so that matching of the luminance delay line is very easy.
It also incorporates the following functions:

- d.c. contrast control;
- d.c. brightness control;
- black level clamp;
- blanking;
- additional video output with positive-going sync.

The chrominance amplifier comprises:

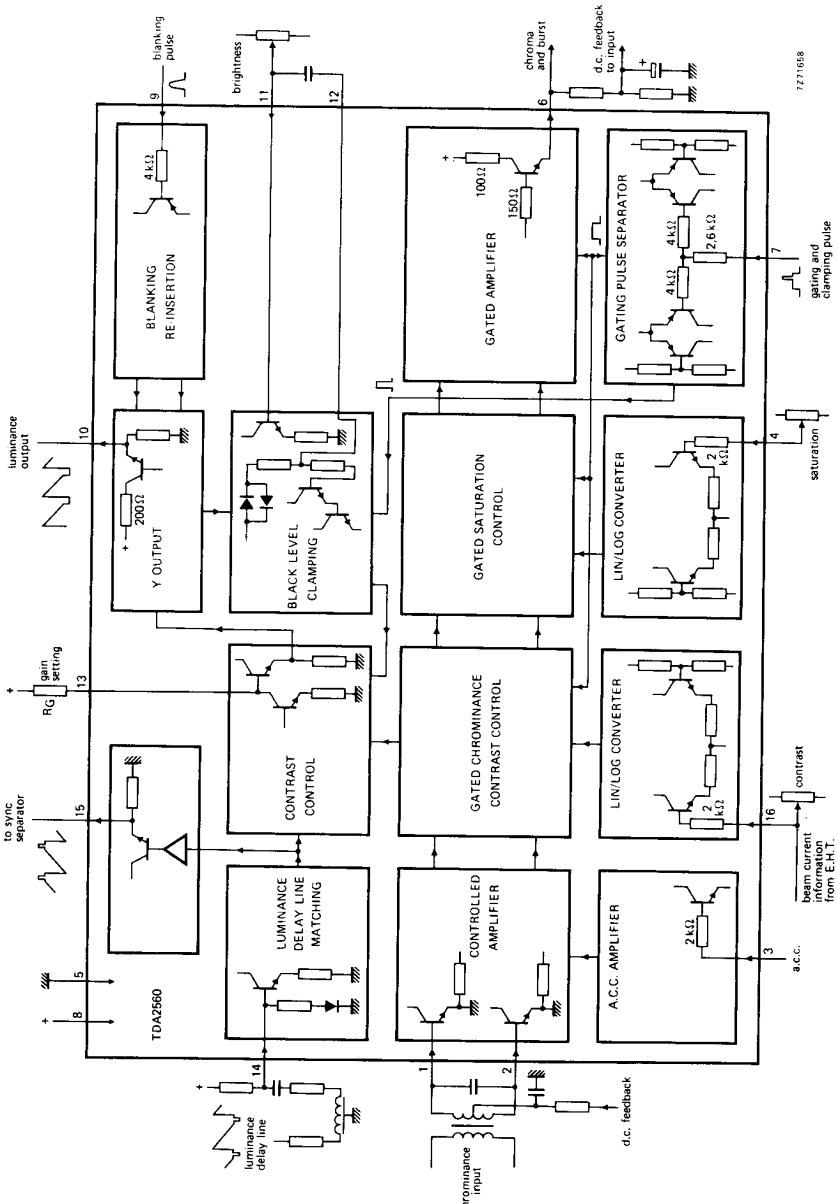
- gain controlled amplifier;
- chrominance gain control tracked with contrast control;
- separate d.c. saturation control;
- combined chroma and burst output, burst signal amplitude not affected by contrast and saturation control;
- the delay line can be driven directly by the IC.

QUICK REFERENCE DATA				
Supply voltage	V_{8-5}	typ.	12	V
Supply current	I_8	typ.	45	mA
Luminance signal input current (black-to-white value)	I_{14}	typ.	0,2	mA
Chrominance input signal (peak-to-peak value)	$V_{2-1(p-p)}$		4 to 80	mV
Luminance output signal at nominal contrast (black-to-white value)	V_{10-5}	typ.	3	V
Chrominance output signal at nominal contrast and saturation and 1,25 V peak-to-peak burst output (peak-to-peak value)	$V_{6-5(p-p)}$	typ.	2,5	V
Contrast control range		>	20	dB
Saturation control range		>	20	dB

PACKAGE OUTLINES

TDA2560 : 16-lead DIL ; plastic (SOT-38).
TDA2560Q: 16-lead QIL ; plastic (SOT-58).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltage				
Supply voltage	V_{8-5}	max.	14	V
Power dissipation				
Total power dissipation	P_{tot}	max.	930	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +65	°C

CHARACTERISTICS measured in the circuit on page 7

Supply voltage range	V_{8-5}	typ.	12	V
			10 to 14	V
Supply current	I_8	typ.	45	mA[1])
Allowable hum on supply line (peak-to-peak value)	$V_{8-5(p-p)}$	<	100	mV

The following data are measured at V_{8-5} = 12 V; T_{amb} = 25 °C; R_G = 2,7 kΩ

Luminance amplifier

Input signal current: black-to-white value	I_{14}	typ.	0,2	mA
Input bias current	I_{14}	typ.	0,25	mA
Input impedance	$\|Z_{14-5}\|$	typ.	150	Ω[2])
Gain (pin 13)	see note 1 on page 5			
Contrast control range		>	20	dB
Contrast control voltage range	V_{16-5} (see control curve on page 6)			
Contrast control current	I_{16}	<	8	μA
Black level range	V_{10-5}		1 to 3	V
Brightness control voltage range	V_{11-5}	typ.	1 to 3	V
Brightness control current	I_{11}	<	20	μA[3])
Black level stability when changing temperature		typ.	0,1	mV/°C
Black level stability when changing contrast	see page 9 (pin 10)			
Bandwidth (−3 dB)	B	>	5	MHz[4])

1) At a load on pin 6 of 1,5 kΩ, and no load on pins 10 and 15.

2) At an input bias current of 0,25 mA.

3) At V_{11-5} > 4 V.

4) At nominal contrast (max. contrast setting −3 dB).

CHARACTERISTICS (continued)

Output voltage (black-to-white value)	V_{10-5}	typ.	3	V
Output voltage (additional; positive-going sync) peak-to-peak value	$V_{15-5(p-p)}$	typ.	3, 4	V[1]
Black level clamp pulse (see note 2 on page 5)				
on level	V_{7-5}		7 to V_{8-5}	V
off level	V_{7-5}	<	5	V
Blanking pulse (see note 3 on page 5)				
for 0 V on pin 10: on level	V_{9-5}		2, 5 to 4, 5	V
off level	V_{9-5}	<	1, 5	V
for 1, 5 V on pin 10: on level	V_{9-5}		6 to V_{8-5}	V
off level	V_{9-5}	<	4, 5	V
Chrominance amplifier [2]				
Input signal (peak-to-peak value)	$V_{2-1(p-p)}$		4 to 80	mV
Chrominance output signal at nominal contrast and saturation setting (peak-to-peak value)	$V_{6-5(p-p)}$	typ.	2	V[3]
Maximum chrominance output signal	V_{6-5}		4, 6	V
Bandwidth (−3 dB)	B	typ.	6	MHz
Ratio of burst and chrominance at nominal contrast and saturation	see notes 4 and 5 on page 5			
A.C.C. starting voltage (see note 6 on page 5)	V_{3-5}	typ.	1, 2	V
A.C.C. range		>	30	dB
Tracking between luminance and chrominance with contrast control (10 dB control)		typ.	±1	dB
Saturation control range		>	20	dB
Saturation control voltage range	V_{4-5} (see control curve on page 6)			
Gating pulse for chrominance amplifier				
on level	V_{7-5}		2, 3 to 5	V
off level	V_{7-5}	<	1	V
width	t_7	>	8	µs
Signal-to-noise ratio at nominal input voltage	S/N	>	46	dB
Phase shift between burst and chrominance		<	5°	

[1]) For I_{14} = 0, 2 mA (black-to-white value).

[2]) All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chrominance ratio is 1:2.

[3]) At a burst signal of 1 V peak-to-peak; see also notes 4 and 5 on page 5.

NOTES

1. The gain of the luminance amplifier can be adjusted, by setting the gain of the contrast control circuit by selection of discrete resistor R_G (see also circuit on page 7). This circuit configuration has been chosen to reduce the spread of the gain to a minimum (main cause of spread is now the spread of the ratio of the delay line matching resistors and the resistor R_G). At R_G = 2,7 kΩ the output voltage at nominal contrast (maximum −3 dB) is 3 V black-to-white for an input current of 0,2 mA black-to-white.

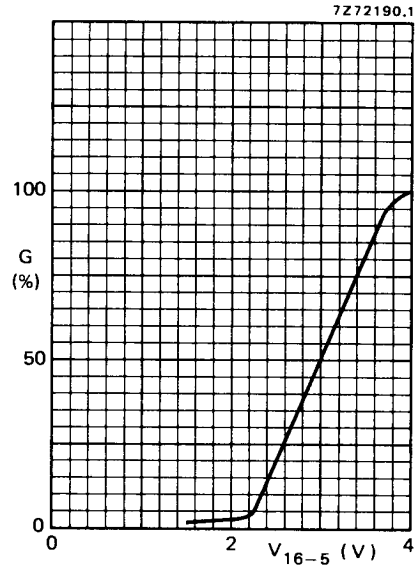
2. This pulse (pin 7) is used for gating of the chrominance amplifier and black level clamping. The latter function is actuated at a +7 V level. The input pulse must have such an amplitude that the clamping circuit is active only during the back porch of the blanking interval. The gating pulse switches the gain of the chroma amplifier to maximum during the flyback time, when the pulse rises above 2,3 V and switches it back to normal setting when the pulse falls below 1 V.

3. This pulse (pin 9) is used for blanking the luminance amplifier. When the pulse exceeds the +2,5 V level the output signal is blanked to a level of about 0 V. When the input exceeds a +6 V level a fixed level of typ. +1,5 V is inserted in the output signal. This level can be used for clamping purposes.

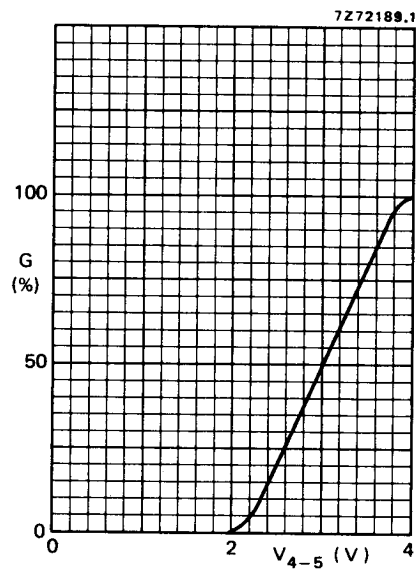
4. The chrominance and burst signal are both available on this pin (6). The burst signal is not affected by the contrast and saturation control and is kept constant by the a.c.c. circuit of the TDA2522. The output of the delay line matrix circuit, which is the input of the TDA2522, is thus automatically compensated for the insertion losses. This means that the output signal of the TDA2560 is determined by the insertion losses of the delay line. At nominal contrast and saturation setting the ratio of burst to chrominance signal at the output is typically identical to that at the input.

5. Nominal contrast is specified as maximum contrast −3 dB. Nominal saturation is specified as maximum saturation −6 dB.

6. A negative-going control voltage gives a decrease in gain.

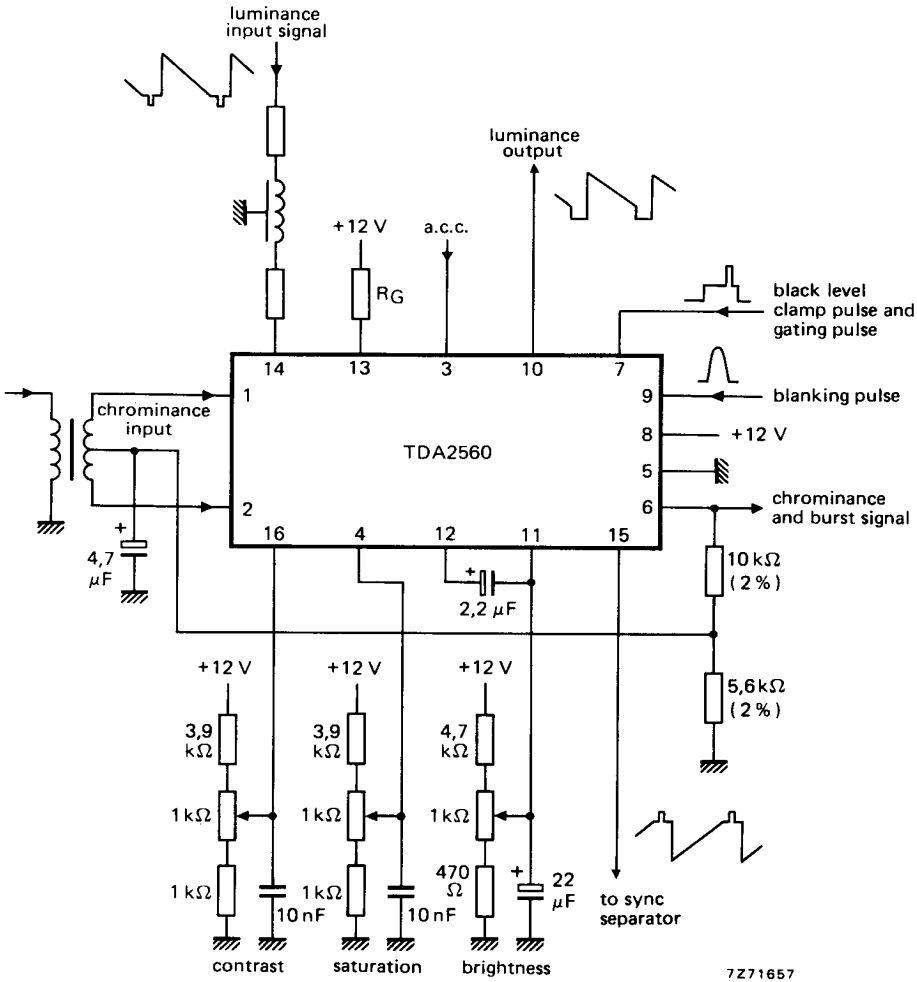


Contrast control of luminance and chrominance amplifier



Saturation control of chrominance amplifier

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Balanced chrominance input signal (in conjunction with pin 2)

   This is derived from the chrominance signal bandpass filter, designed to provide a push-pull input. A signal amplitude of at least 4 mV peak-to-peak is required between pins 1 and 2. The chrominance amplifier is stabilized by an external feedback loop from the output (pin 6) to the input (pins 1 and 2). The required level at pins 1 and 2 will be 3 V.
   All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chrominance ratio of input signal is 1 : 2.

2. Chrominance signal input (see pin 1)

3. A.C.C. input

   A negative-going potential, starting at +1,2 V, gives a 40 dB range of a.c.c. Maximum gain reduction is achieved at an input voltage of 500 mV.

4. Chrominance saturation control

   A control range of +6 dB to >−14 dB is provided over a range of d.c. potential on pin 4 from +2 to +4 V. The saturation control is a linear function of the control voltage.

5. Negative supply (earth)

6. Chrominance signal output

   For nominal settings of saturation and contrast controls (max. −6 dB for saturation, and max. −3 dB for contrast) both the chroma and burst are available at this pin, and in the same ratio as at the input pins 1 and 2. The burst signal is not affected by the saturation and contrast controls. The a.c.c. circuit of the TDA2522 will hold constant the colour burst amplitude at the input of the TDA2522. As the PAL delay line is situated here between the TDA2560 and TDA2522 there may be some variation of the nominal 1 V peak-to-peak burst output of the TDA2560, according to the tolerances of the delay line. An external network is required from pin 6 of the TDA2560 to provide d.c. negative feedback in the chroma channel via pins 1 and 2.

7. Burst gating and clamping pulse input

   A two-level pulse is required at this pin to be used for burst gate and black level clamping. The black level clamp is activated when the pulse level is greater than 7 V. The timing of this interval should be such that no appreciable encroachment occurs into the sync pulse on picture line periods during normal operation of the receiver. The burst gate, which switches the gain of the chroma amplifier to maximum, requires that the input pulse at pin 7 should be sufficiently wide, at least 8 μs, at the actuating level of 2,3 V.

APPLICATION INFORMATION (continued)

8. +12 V power supply

Correct operation occurs within the range 10 to 14 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels.

9. Flyback blanking input waveform

This pin is used for blanking the luminance amplifier. When the input pulse exceeds the +2, 5 V level, the output signal is blanked to a level of about 0 V. When the input exceeds a +6 V level, a fixed level of about 1, 5 V is inserted in the output. This level can be used for clamping purposes.

10. Luminance signal output

An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 1 to 3 V. An external emitter load resistor is not required.
The luminance amplitude available for nominal contrast may be modified according to the resistor value from pin 13 to the +12 V supply. At an input bias current I_{14} of 0, 25 mA during black level the amplifier is compensated so that no black level shift more than 10 mV occurs at contrast control. When the input current deviates from the quoted value the black level shift amounts to 100 mV/mA.

11. Brightness control

The black level at the luminance output (pin 10) is identical to the control voltage required at this pin. A range of black level from 1 to 3 V may be obtained.

12. Black level clamp capacitor

13. Luminance gain setting resistor

The gain of the luminance amplifier may be adjusted by selection of the resistor value from pin 13 to +12 V. Nominal luminance output amplitude is then 3 V black-to-white at pin 10 when this resistor is 2, 7 kΩ and the input current is 0, 2 mA black-to-white. Maximum and minimum values of this resistor are 3, 9 kΩ and 1, 8 kΩ.

14. Luminance signal input

A low input impedance in the form of a current sink is obtained at this pin. Nominal input current is 0, 2 mA black-to-white. The luminance signal may be coupled to pin 14 via a d.c. blocking capacitor and, in addition, a resistor employed to give a d.c. current into pin 14 at black level of about 0, 25 mA. Alternatively d.c. coupling from a signal source such as the TDA2540 and TDA2541 may be employed.

APPLICATION INFORMATION (continued)

15. Luminance signal output for sync separator purposes

A luminance signal output with positive-going sync is available which is not affected by the contrast control or the value of resistor at pin 13. This voltage is intended for drive of sync separator circuits. The output amplitude is 3, 4 V peak-to-peak when the luminance signal input is 0, 2 mA black-to-white.

16. Contrast control

With 3 V on this pin the gain of the luminance channel is such that 0, 2 mA black-to-white at pin 14 gives a luminance output on pin 10 of 3 V black-to-white. The nominal value of 2, 7 kΩ is then assumed for the resistor from pin 13 to the +12 V supply. The variation of control potential at pin 16 from 2 to 4 V gives −17 to +3 dB gain variation of the luminance channel. A similar variation in the chrominance channel occurs in order to provide correct tracking between the two signals.