DATA SHEET

SAA7280
Terrestrial Digital Sound Decoder (TDSD)

Preliminary specification
IC01

July 1991

Philips Semiconductors

PHILIPS

Terrestrial Digital Sound Decoder (TDSD)

SAA7280

FEATURES

- Full EBU NICAM 728 specification decoder
- Microcomputer controlled by I²C-bus
- Automatic decoding and output configuration depending upon transmission:
  - digital stereo
  - digital mono and data
  - 2 independent mono signals
- On board RAM for de-interleaving and 10 to 14 bit word expansion
- 7 sample interpolator for erroneous samples
- 3 times digital over-sampling filter (selectable)
- I²S sound bus output format
- I²C-bus transceiver enabling a master device to read:
  - status information
  - error count byte
  - additional data bits

  and write:
  - switch control codes
  - decoder control
- Status information and decoder control available via external pins.

APPLICATIONS

- Television receivers
- Video cassette recorders

GENERAL DESCRIPTION

Performing all digital decoding functions for a NICAM 728 digital stereo sound system, the SAA7280 is a CMOS integrated circuit which operates in conjunction with a DQPSK (Differential Quadrature Phase Shift Keying) demodulator (TDA8732) and a dual DAC (TDA1543). The device may also be interfaced to other DQPSK demodulators and DACs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	4.5	5.0	5.5	V
I_{DD}	supply current	-	50	-	mA
f_{XTAL}	crystal frequency	-	17.472	-	MHz
T_{amb}	operating ambient temperature	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7280P	28	DIL	plastic	SOT117

PIN CONFIGURATION

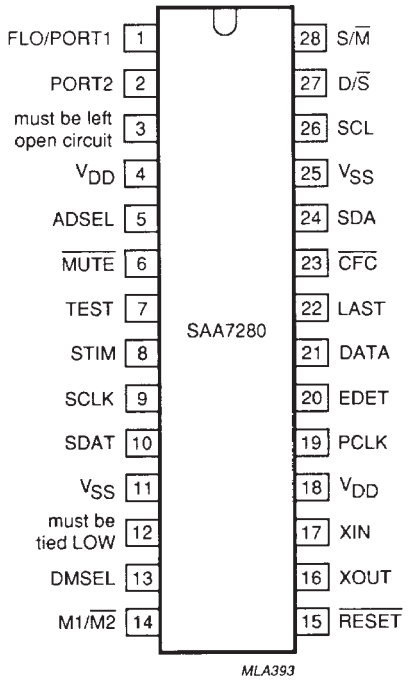


Fig.1 Pin configuration.

BLOCK DIAGRAM

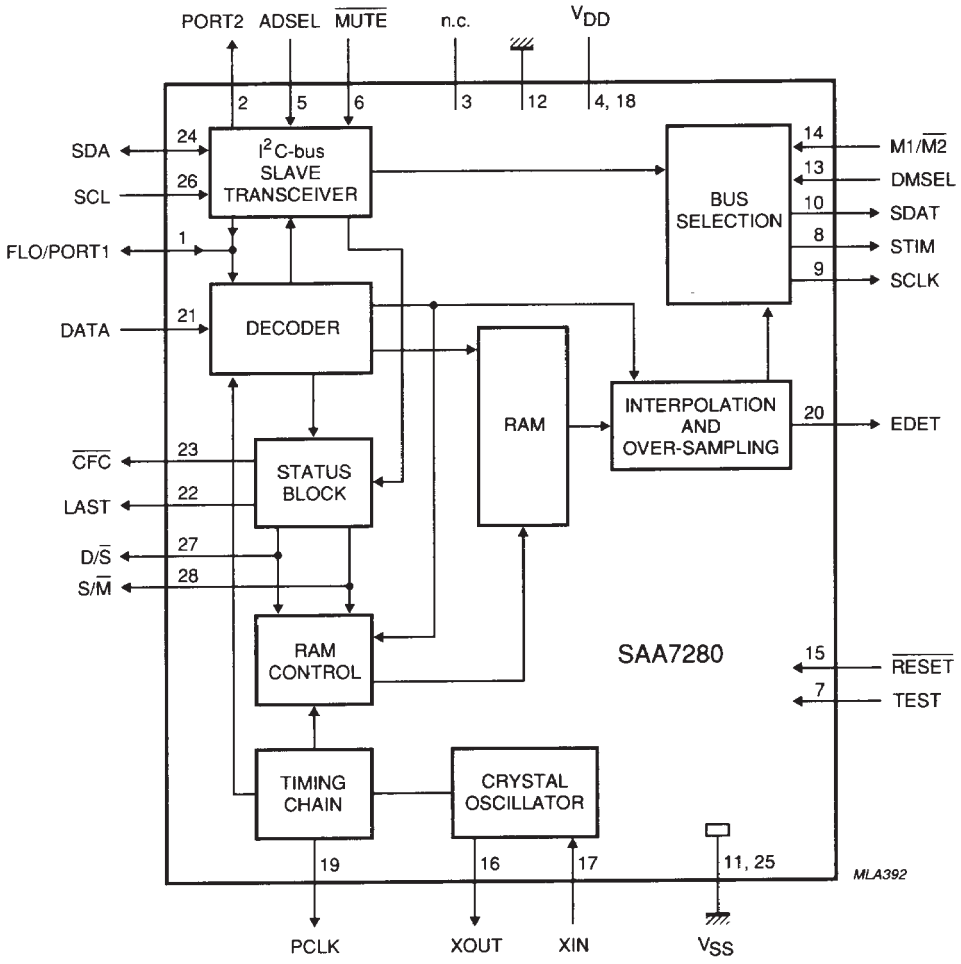


Fig.2 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FLO/PORT1	1	I/O reserve sound switching flag override when selected as an input which is used in the logical equation for the 'LAST' output. Defaults to an input but can be set by control of the I²C-bus. Becomes a port output pin when selected by PT1EN bit in the I²C-bus of the control register with control via bit PORT1.
PORT2	2	provides an output port controlled by bit PORT2 via the I²C-bus interface control register. (See Fig.3)
n.c.	3	not used; must be left open-circuit.
V_{DD}	4, 18	+5 V power supply
ADSEL	5	I²C-bus slave address selection input. Allows selection of one of two separate slave addresses.

ADSEL	TDSD Slave Address							
	A6	A5	A4	A3	A2	A1	A0	R/W
HIGH	1	0	1	1	0	1	1	X
LOW	1	0	1	1	0	1	0	X

$\overline{MUTE}$	6	when asserted will mute the SDAT output samples. Sets sample values to zero. Input is active LOW in non-I²C-bus applications. With I²C-bus active, mute polarity can be set by SC3 bit to 'exclusive-OR' operation (see Fig. 3).
TEST	7	normally connected to V_{SS}.
STIM	8	sound bus output timing signal (I²S word selection).
SCLK	9	sound bus output clock (I²S clock).
SDAT	10	sound bus data output pin (I²S data).
V_{SS}	11, 25	ground (0 V).
n.c.	12	not used. Must be tied LOW.
DMSEL	13	active HIGH 'dual mono selection' input. Selects M1 and M2 as the output signals when the incoming transmission comprises two independent mono signals.
M1/$\overline{M2}$	14	'M1' (M1/$\overline{M2}$ = 1) or 'M2' (M1/$\overline{M2}$ = 0) selection input when the input transmission consists of two independent mono signals (see Fig. 3).
$\overline{RESET}$	15	active LOW reset input to initialise device (e.g. at power-up).
XOUT	16	respectively, the output and input of a single stage inverter used to provide a crystal oscillator maintaining circuit (with external biassing) or a simple CMOS input at XIN for the 17.472 MHz
XIN	17	master clock
PCLK	19	728 kHz clock output derived from 17.472 MHz crystal.
EDET	20	active HIGH error detection output.
DATA	21	serial data at 728 Kbits/s from DQPSK demodulator.

<table>
<tr><th>SYMBOL</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>LAST</td><td>22</td><td>logic 'AND' status providing status of VDSP.(RSSF+FLO) (see Fig 3).
VDSP, "valid digital sound present" signal. When HIGH this output indicates that the decoder is operating with a valid NICAM digital input which carries at least one sound channel. RSSF "or" FLO.
FLO is a RSSF override signal which allows a user to turn off the RSSF input to the 'LAST' function. The purpose of this is to disable the RSSF input to the logical AND status pin (LAST) thus allowing the user to determine whether there is a reserve sound switching capability when the decoder is out of sync or receiving 'transparent data'.
RSSF is a signal which indicates the reserve sound switching status. When HIGH this output shows that the conventional analogue FM signal is the same as the digital signal being decoded. Thus a failure of the digital signal can result in the circuit switching to conventional analogue sound.
<table>
<tr><th>VDSP</th><th>RSSF</th><th>FLO</th><th>LAST</th><th></th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>0</td><td rowspan="4">Where 'X' denotes "don't care"</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>X</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>$\overline{CFC}$</td><td>.23</td><td>active LOW open drain output. Signifies a change of configuration at the 16-frame boundary (not 8 ms in advance). Cleared after 128 ms time out (non-I²C-bus applications) or by the I²C-bus reading the status register.</td></tr>
<tr><td>SDA</td><td>24</td><td>I²C-bus data input/open drain input.</td></tr>
<tr><td>SCL</td><td>26</td><td>I²C-bus clock input. (Maximum speed 100 kHz).</td></tr>
<tr><td>D/$\overline{S}$</td><td>27</td><td>output pin indicating single or dual mono sound: D/$\overline{S}$ = 1 indicates dual mono; D/$\overline{S}$ = 0 indicates not dual mono. This bit is also available within the I²C-bus register map.</td></tr>
<tr><td>S/$\overline{M}$</td><td>28</td><td>output pin providing indication of the presence of mono or stereo sound. S/$\overline{M}$ = 1 indicates stereo; S/$\overline{M}$ = 0 indicates mono. This bit is also available within the I²C-bus register map.</td></tr>
</table>

I²C-bus FORMATS

The SAA7280 contains an I²C-bus slave transceiver permitting a master device to:-

- Read decoder status information derived from the transmitted digital audio signal
- Read an error count byte to determine the bit error rate for mute purposes
- Read additional transmitted data bits. Their purpose has yet to be defined but accessibility is provided to allow future services to be implemented in receiver software
- Write control codes to select the available analogue switching configurations
- Select the output configuration by writing control information to the device.

The device slave address is A(6:0)(R/W) = 101101X(R/W). An ADSEL pin is provided to allow selection of one of two different slave addresses via programmable address bit A0.

The SAA7280 does not acknowledge the I²C-bus general call address.

The slave receiver format is:

S SLAVE_ADDR.0 ACK SUB_ADDR ACK $\frac{\textit{DATA BYTE ACK}}{[\textit{.....n bytes.....}]}$ *P*

Auto-increment of the sub-address is provided with wrap-around from 0F (HEX) to 00 (HEX).

The slave receiver data byte format, as a function of sub-address, is as follows:

The functions of these bits is as follows:

SUB_ADDRESS	RESET VALUE	D7	D6	D5	D4	D3	D2	D1	D0
01	09	M1/$\overline{M2}$	DMSEL	$\overline{OVS}$	SC3	SBEN	PORT2	PT1EN	PORT1

M1/$\overline{M2}$

This bit selects either M1 (M1/$\overline{M2}$ = 1) or M2 (M1/$\overline{M2}$ = 0) when the input transmission consists of two independent mono signals (see Fig. 3).

DMSEL

DMSEL is the dual mono selection bit. When asserted it selects M1 and M2 as the output signals if the incoming transmission consists of two independent mono signals.

The M1/$\overline{M2}$ and DMSEL bits are exclusive-ORed with the dedicated M1/$\overline{M2}$ and DMSEL pins respectively. By setting the appropriate pins or bits LOW, this allows the source of these signals to be from either the I²C-bus or input pins (see Fig. 3).

$\overline{OVS}$

Forming the active LOW over-sampling selection bit, $\overline{OVS}$ selects between x3 over-sampled output ($\overline{OVS}$ = 0) and non over-sampled output ($\overline{OVS}$ = 1). The default format is for over-sampled output ($\overline{OVS}$ = 0).

SC3

This bit selects the polarity of the external MUTE pin.

SC3 = 1 = > external MUTE is active HIGH
SC3 = 0 = > external MUTE is active LOW

Note that the external MUTE facility overrides in all modes and by default is actively LOW in the I²C-bus free mode.

SBEN

SBEN is the sound bus enable bit. The default condition enables the sound bus (SBEN = 1).

PORT2

PORT2 controls a bit out, providing direct access to a dedicated output pin (P2) via the I²C-bus (see Fig.3).

DMSEL	M1/$\overline{M2}$	FUNCTION
0	0	selects DIGITAL, L = M2 R = M2
0	1	selects DIGITAL, L = M1 R = M1
1	0	selects DIGITAL, L = M1 R = M2
1	1	selects DIGITAL, L = M2 R = M1

PORT2	PORT2 CONTROL OUTPUT STATE
0	LOW
1	HIGH

PT1EN

This is an actively HIGH, PORT1 enable signal. It is used to force the FLO/PORT1 pin to an input or an output.

PT1EN	FLO/PORT1 PIN
1	OUTPUT
0	INPUT

PORT1

PORT1 Controls a bit out, providing direct access to a dedicated output pin (PORT1) via the I²C-bus (see Fig.3).

PORT1	PORT1 CONTROL OUTPUT STATE
0	LOW
1	HIGH

Slave Transmitter

The slave transmitter formats are illustrated thus:

Where S = start, A = acknowledge, P = stop.

a) S SLAVE_ADDR.1 A STATUS_BYTE NA P

In this format the bus master reads the STATUS_BYTE once. This format is compatible with the status read from the TDA8405.

b) S SLAVE_ADDR.1 A STATUS_BYTE A ERROR_BYTE NA P

In this format the bus master reads two bytes of STATUS_BYTE and ERROR_BYTE.

c) S SLAVE_ADDR.1 A STATUS_BYTE A ERROR_BYTE A AD_BYTE_0 A AD_BYTE_1 NA P

In this format the bus master reads four bytes of STATUS_BYTE, ERROR BYTE and two additional bytes, AD_BYTE_0 and AD_BYTE_1. The additional data bytes contain the eleven additional data bits AD0 to AD10 together with information regarding their status.

The bits may be defined as follows:-

PONRES
is a power-on reset detection bit. It is set HIGH after a power-on reset or supply reduction and is cleared LOW when the STATUS_BYTE is read.

S/$\overline{M}$
stereo/mono indication:

S/$\overline{M}$ = 1 indicating an incoming stereo transmission
S/$\overline{M}$ = 0 indicating that the incoming transmission is not stereo.

D/$\overline{S}$
dual/single mono indication:

D/$\overline{S}$ = 1 indicating an incoming dual mono transmission
D/$\overline{S}$ = 0 indicating that the incoming transmission is not dual mono.

VDSP
indicates that the decoded signal is valid digital sound. When VDSP = 0 the incoming transmission carries either a 704 Kbit/s transparent data

DATA BYTE FORMATS

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
STATUS_BYTE	PONRES	S/$\overline{M}$	D/$\overline{S}$	RSSF	VDSP	$\overline{OS}$	LAST	$\overline{CFC}$
ERROR_BYTE	E7	E6	E5	E4	E3	E2	E1	E0
AD_BYTE_0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
AD_BYTE_1	OVW	SAD	0	CI2	CI1	AD10	AD9	AD8

INDICATOR BITS FUNCTIONAL TRUTH TABLE

TRANSMISSION	C1	C2	C3	S/$\overline{M}$	D/$\overline{S}$	VDSP	$\overline{OS}$
STEREO	0	0	0	1	0	1	1
M1 + M2	0	1	0	0	1	1	1
M1 + DATA	1	0	0	0	0	1	1
TRANS. DATA	1	1	0	0	0	0	1
ANY CURRENTLY UNDEFINED COMBINATION OF C1, C2, C3				0	0	0	1
DECODER UNSYNCHRONIZED ($\overline{OS}$ = 0)				0	0	0	0

channel or a currently undefined format is being received.

RSSF
is the reserve sound switching flag indication equal to the C4 bit in the NICAM transmission. RSSF = 1 when the FM sound signal is carrying the same programme material as the digitally modulated carrier (specifically the M1 signal in the case of a dual mono transmission). RSSF = 0 when the FM signal is not reproduced within the digital signal.

$\overline{OS}$
provides an active LOW indication that the decoder is out of sync. If $\overline{OS}$ = 1 the decoder is frame synchronized and has obtained CO (16 frame) sync. If $\overline{OS}$ = 0, the decoder is out of sync. and the indicator bits are as given in the truth table.

LAST
is the logical AND of VDSP and RSSF 'OR' FLO, i.e. LAST = VDSP.(RSSF + FLO). It provides an I²C-bus indicator regarding the status of the output pin LAST.

$\overline{CFC}$
signals a change of configuration at the 16-frame boundary. It is cleared to '1' by the I²C-bus reading the status register or after 128 ms time out for non-I²C-bus applications.

E7-E0
is an error count byte which counts the number of error flags. The maximum count (255) is held, becomes invalid and is cleared when it is read by the I²C-bus status register.

AD10-AD0
are the additional data bits from the transmission and are updated every 1 ms. This provides a data capacity of 11 Kbit/s.

SAD
is the 'status additional data' bit. This is set to '1' when new bits AD10-AD0 are latched into the I²C-bus registers. It is automatically reset to '0' when AD_BYTE_1 is read by the bus master.

OVW
is the overwrite indicator for the additional data. This bit is set as new additional data bits are latched into the I²C-bus registers when SAD = 1, i.e. when the transmission overwrites additional data bits which have not been read by the bus master. This bit is automatically reset to '0' when AD_BYTE_1 is read by the bus master.

CI1-CI2
represent the CIB bits which are extracted by a majority logic process from the parity checks of the last ten samples in a frame (samples 55 to 64). CI1 will be conveyed by the parity grouping of samples 55 to 59 and CI2 will be conducted by the parity grouping of samples 60 to 64. Both parity groups will be even for UK transmissions such that CI2 = 0 and CI1 = 0. The transmissions of countries following the specification issued by the EBU (Doc. SPB424; Digital sound transmissions in terrestrial television) will allow odd or even parity groups, thus providing an additional 2 Kbit/s data capacity.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	+6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage	−0.3	V_{DD}+0.5	V
V_{stat}	electrostatic handling *	−2000	+2000	V
I_{IOK}	DC input or output diode current	-	±20	mA
IO_{max}	output current (each output)	-	±10	mA
T_{amb}	ambient operating temperature	0	+70	° C
T_{stg}	storage temperature range	−30	+125	° C

Note

* Electrostatic handling ratings equivalent to discharging a pulse with a 15 ns rise time from a 100 pF capacitor through a 1.5 kΩ resistor.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to +70 ° C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	V_{SS} = 0 V	4.5	5	5.5	V
Inputs $\overline{\text{RESET}}$						
V_{T+}	positive going threshold	Schmitt trigger	2.2	-	-	V
V_{T-}	negative going threshold	Schmitt trigger	-	-	0.8	V
TEST, ADSEL, DATA, $\overline{\text{MUTE}}$, DMSEL, M1/M2 and FLO/PORT1						
V_{IH}	input voltage HIGH		2	-	V_{DD}+0.5V	V
V_{IL}	input voltage LOW		0	-	0.8	V
C_I	input capacitance		-	-	10	pF
SDA and SCL						
V_{IH}	input voltage HIGH		0.7V_{DD}	-	V_{DD}+0.5V	V
V_{IL}	input voltage LOW		0	-	0.3V_{DD}	V
C_I	input capacitance		-	-	10	pF
XIN and XOUT (crystal oscillator)						
gm	transconductance		-	-	12	mA/V
Av	small signal gain	at 25 MHz	-	7.2	-	-
C_I	input capacitance		-	10	-	pF
C_{FB}	feedback capacitance		-	5	-	pF
C_O	output capacitance		-	10	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs SDAT, STIM, SCLK, PCLK and EDET						
V_{OH}	output voltage HIGH	I_O = −2 mA	2.4	-	-	V
V_{OL}	output voltage LOW	I_O = 2 mA	-	-	0.4	V
C_L	load capacitance		-	-	50	pF
S/$\overline{M}$, D/S, LAST, $\overline{PORT2}$ and FLO/$\overline{PORT1}$						
V_{OH}	output voltage HIGH	I_O = - 4 mA	2.4	-	-	V
V_{OL}	output voltage LOW	I_O = 4 mA	-	-	0.4	V
C_L	load capacitance		-	-	50	pF
$\overline{CFC}$						
V_{OL}	output voltage LOW	I_O = 4 mA	-	-	0.4	V
C_L	load capacitance		-	-	50	pF
SDA						
V_{OL}	output voltage LOW	I_O = 4mA	-	-	0.4	V
C_L	load capacitance		-	-	400	pF
Timing						
f_{XTAL}	crystal operating frequency		15.725	17.472	19.219	MHz
Timing of inputs: data with respect to PCLK						
t_{SU}	set-up time		100	-	-	ns
t_{HD}	hold time		100	-	-	ns
SDA and SCL (see Fig. 5)						
f_{SCL}	operating frequency		1	-	100	kHz
t_r	input rise time		-	-	1	µs
t_f	input fall time		-	-	300	ns
t_{BUF}	bus free time		4	-	-	µs
t_{LOW}	SCL LOW time		4	-	-	µs
t_{HIGH}	SCL HIGH time		4	-	-	µs
$t_{SU;STA}$	start code set-up time		4	-	-	µs
$t_{HD;STA}$	start code hold time		4	-	-	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	stop code set-up time		4	-	-	µs
t_{CYC}	SCL cycle time		10	-	-	µs
Timing of outputs: SDA						
t_{OH}	hold time		250	-	-	ns
t_{OD}	delay time		-	-	3	ns
SDAT, STIM and SCLK						
t_r/t_f	rise/fall time		-	-	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCLK I²S over-sampled output (see Figs. 6 and 7)						
t_{CK}	clock period		-	343	-	ns
t_{CKH}	clock HIGH time		-	172	-	ns
t_{CKL}	clock LOW time		-	172	-	ns
SCLK I²S non over-sampled output						
t_{CK}	clock period	see note 1	1.03	-	1.2	µs
t_{CKH}	clock HIGH time		-	515	-	ns
t_{CKL}	clock LOW time		515	-	687	ns
SDAT, STIM with respect to SCLK (see Fig. 7)						
t_{SU}	set-up time		40	-	-	ns
t_{HD}	hold time		5	-	-	ns
PCLK						
t_{CK}	clock period		1.3	1.37	-	µs
t_{CKH}	clock HIGH time		650	687	-	ns
t_{CKL}	clock LOW time		650	687	-	ns
t_r/t_f	rise/fall time		-	-	20	ns

Note

The clock period for SCLK in I²S non over-sampled mode alternates between 1.03 µs and 1.2 µs.

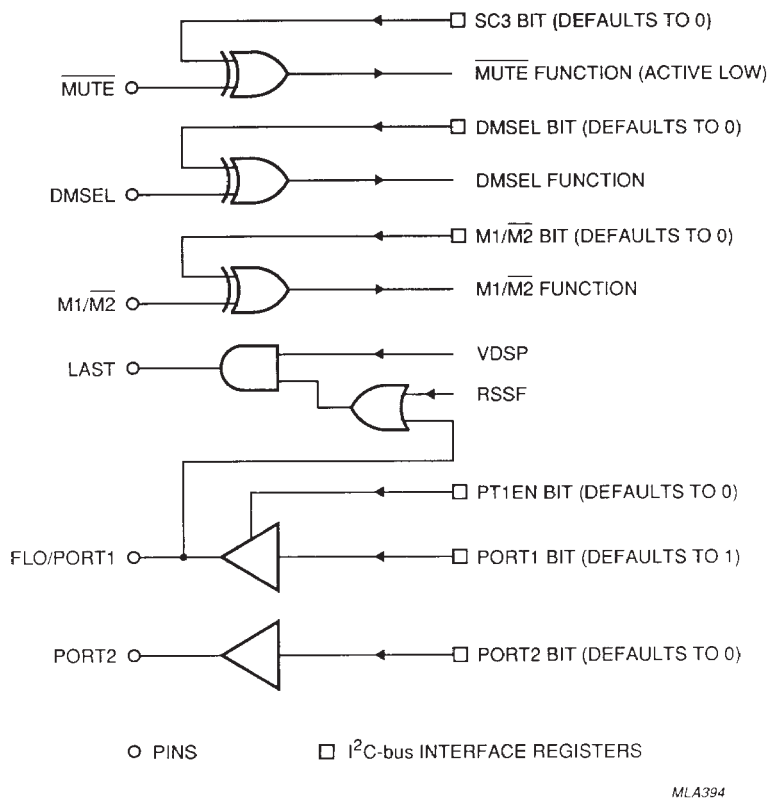


Fig.3 Conceptual diagram of SAA7280 control functions and ports.

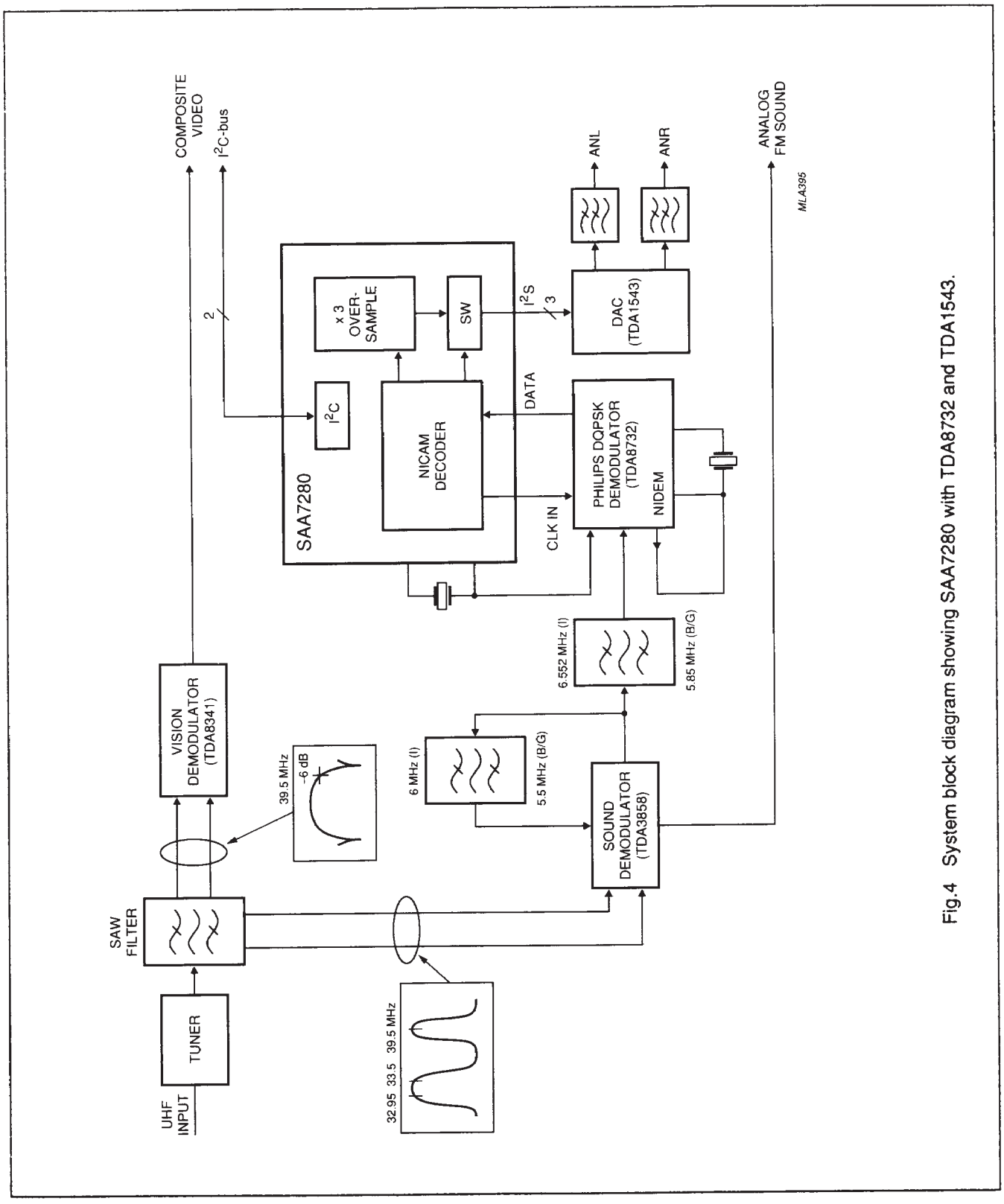


Fig.4 System block diagram showing SAA7280 with TDA8732 and TDA1543.

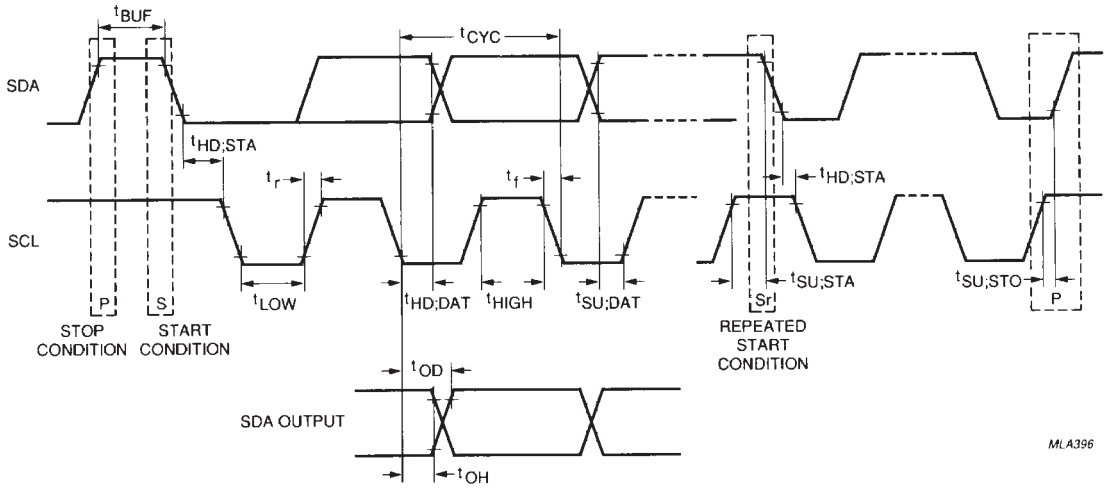
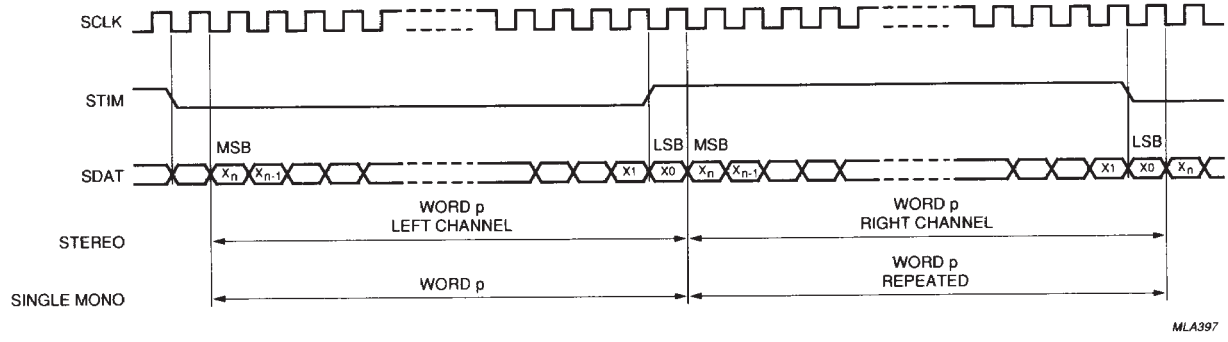


Fig.5 I²C-bus interface timing.



In I²S over-sampled mode there are 15 bits per channel, i.e. n = 14

In I²S non over-sampled mode there are 14 bits per channel, i.e. n = 13

Fig.6 I²S-bus output timing.

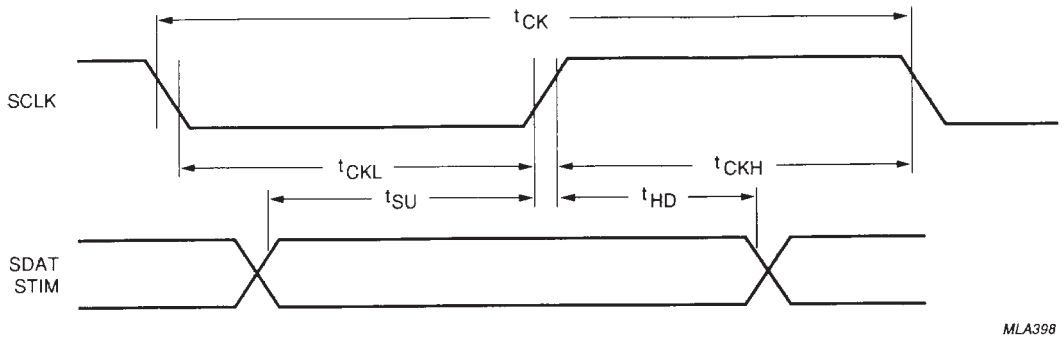


Fig.7 Data output timing.

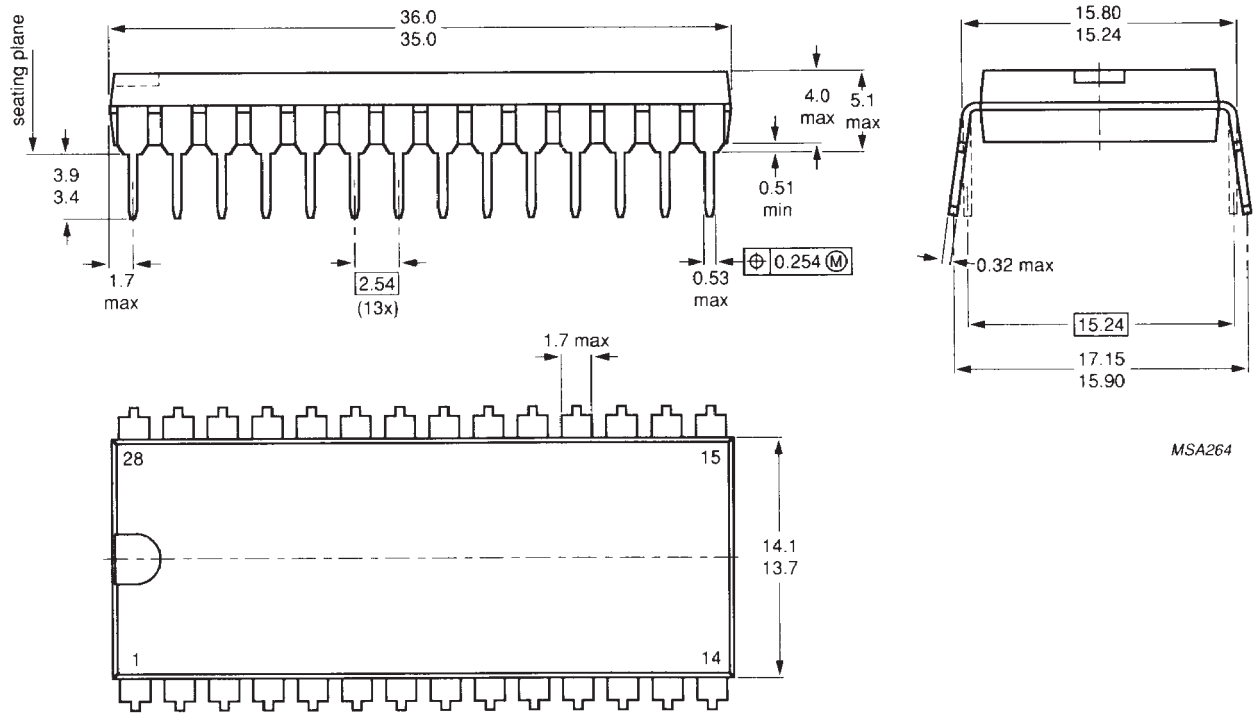


Fig.8 28-lead dual in-line plastic; (SOT117)

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	

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