Signetics

74173, LS173
Flip-Flops

Quad D-Type Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES

- **Edge-triggered D-type register**
- **Gated Input enable for hold "do nothing" mode**
- **3-State output buffers**
- **Gated output enable control**
- **Pin compatible with the 8T10 and DM8551**

DESCRIPTION

The '173 is a 4-bit parallel load register with clock enable control, 3-State buffered outputs and master reset. When the two Clock Enable ($\overline{E}_1$ and $\overline{E}_2$) inputs are LOW, the data on the D inputs is loaded into the register synchronously with the LOW-to-HIGH Clock (CP) transition. When one or both $\overline{E}$ inputs are HIGH one set-up time before the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and Clock Enable inputs are fully edge triggered and must be stable only one set-up time before the LOW-to-HIGH clock transition.

The Master Reset (MR) is an active HIGH asynchronous input. When the MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74173	35MHz	50mA
74LS173	50MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74173N, N74LS173N
Plastic SO-16	N74LS173D
Plastic SOL-16	CD7186D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

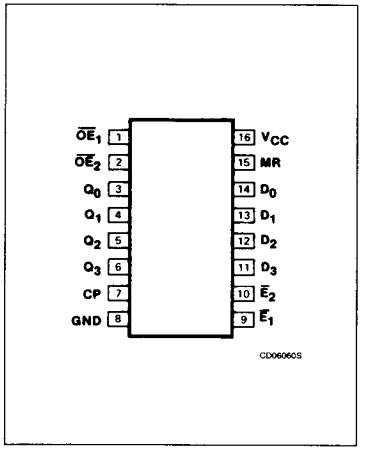
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	30LSul

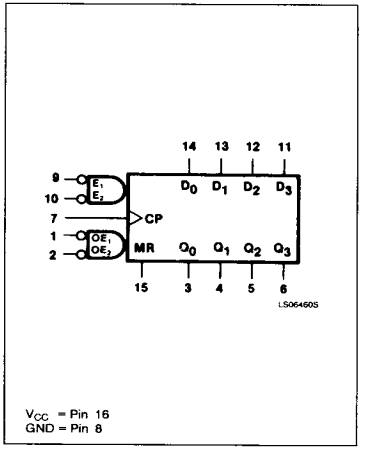
NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_1$ and $\overline{OE}_2$) inputs are LOW, the data in the register is presented at the Q outputs. When one or both $\overline{OE}$ inputs is HIGH, the outputs are forced to a HIGH impedance "off" state. The 3-State output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

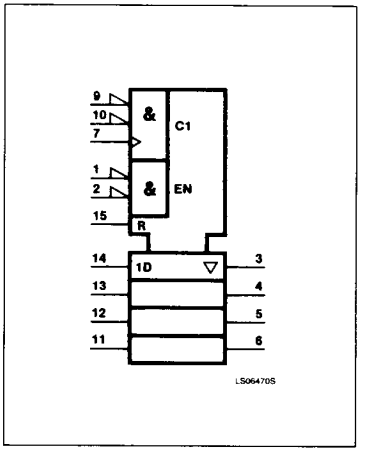
PIN CONFIGURATION



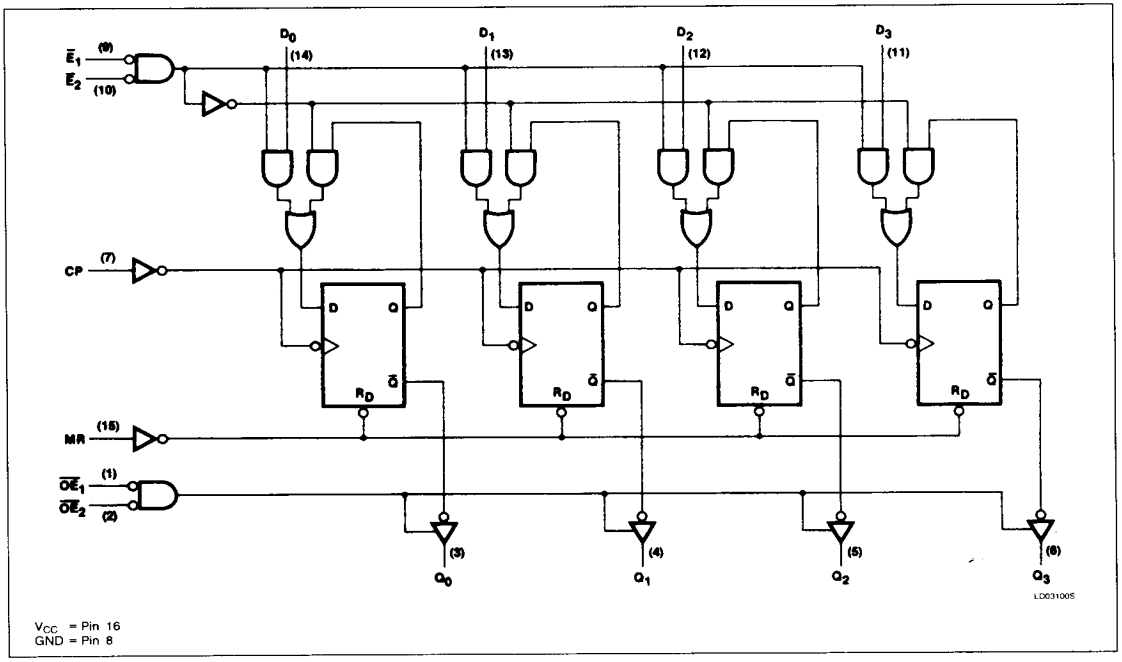
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

MODE SELECT — FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS
	Q_n (Register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0, Q_1, Q_2, Q_3
Read	L	L	L	L
	H	L	L	H
Disabled	X	H	X	(Z)
	X	X	H	(Z)

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced input (or output) on set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
(Z) = HIGH impedance "off" state.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18	mA
I_{OH}	HIGH-level output current			5.2			−2.6	mA
I_{OL}	LOW-level output current			16			24	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74173			74LS173			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.4			2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX			0.4		0.35	0.5	V
			I_{OL} = 12mA (74LS)					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5			−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.4V			40				μA
			V_O = 2.7V						20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V				−40			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V			40				μA
			V_I = 2.7V						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−1.6			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−30		−70	−30		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			50	72		20	30	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V, and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with MR grounded following momentary connection to 4.5V, $\overline{OE}_2$, $\overline{E}_1$, $\overline{E}_2$ and all Data inputs grounded, CP and $\overline{OE}_1$ at 4.5V, and all outputs open.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

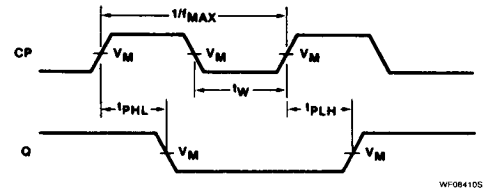
PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 50pF$, $R_L = 400\Omega$		$C_L = 45pF$, $R_L = 667\Omega$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		43 31		25 30	ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		27		35	ns
t_{PZH}	Output enable to HIGH level	Waveform 2		30		23	ns
t_{PZL}	Output enable to LOW level	Waveform 3		30		27	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, $C_L = 5pF$		14		17	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, $C_L = 5pF$		20		17	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

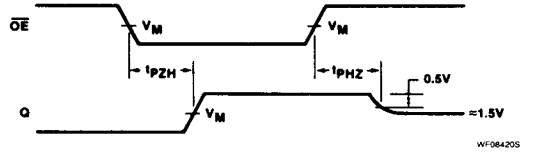
AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
$t_W(CP)$	Clock pulse width	Waveform 1	20		20		ns
$t_W(MR)$	MR pulse width	Waveform 4	20		20		ns
$t_s(D)$	Set-up time, data to clock	Waveform 5	10		17		ns
$t_h(D)$	Hold time, data to clock	Waveform 5	10		0		ns
$t_s(\overline{E})$	Set-up time, enable to clock	Waveform 5	17		35		ns
$t_h(\overline{E})$	Hold time, enable to clock	Waveform 5	2		0		ns
$t_{rec}(MR)$	Recovery time, Master Reset to clock	Waveform 4	10		17		ns

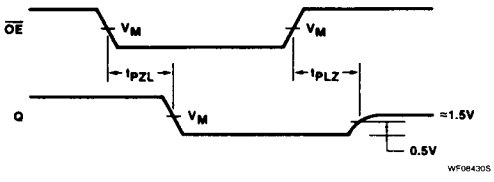
AC WAVEFORMS



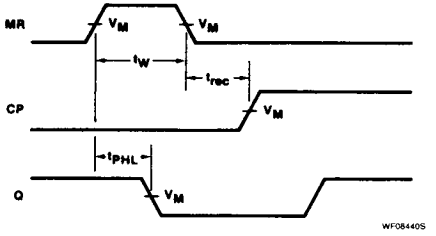
Waveform 1. Clock To Output Delays And Clock Pulse Width



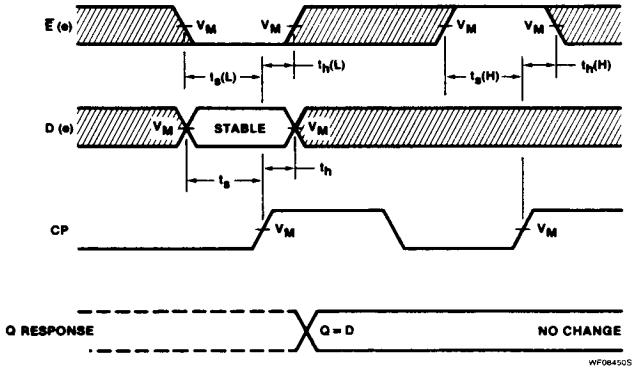
Waveform 2. 3-State Enables Time To HIGH Level And Disable Time From HIGH Level



Waveform 3. 3-State Enable Time To LOW Level And Disable Time From LOW Level



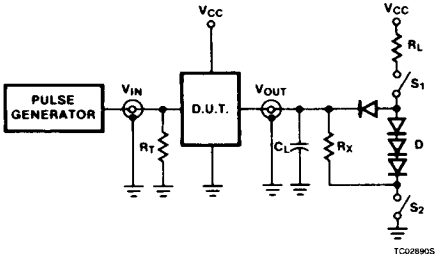
Waveform 4. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



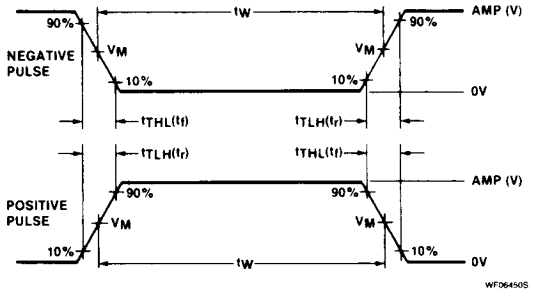
For all waveforms, V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicates when the input is permitted to change for predicable output performances.

Waveform 5. Set-up (t_s) And Hold (t_h) Times Width For Data (D) And Enable (E) Inputs

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

5