

1/54LS/74LS379 011546
54LS/74LS379
QUAD PARALLEL REGISTER
 (With Enable)

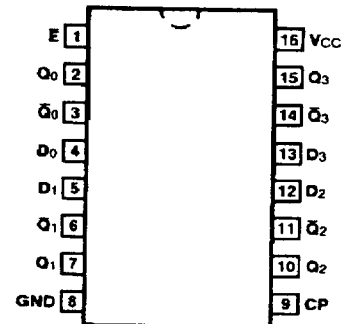
DESCRIPTION — The '379 is a 4-bit register with buffered common Enable. This device is similar to the '175 but features the common Enable rather than common Master Reset.

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- BUFFERED COMMON ENABLE INPUT
- TRUE AND COMPLEMENT OUTPUTS

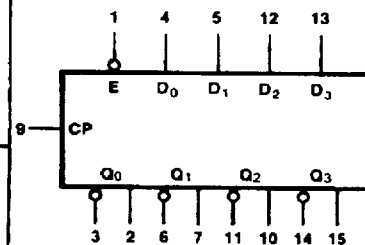
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74LS379PC		9B
Ceramic DIP (D)	A	74LS379DC	54LS379DM	6B
Flatpak (F)	A	74LS379FC	54LS379FM	4L

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
 GND = Pin 8




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INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
\bar{E}	Enable Input (Active LOW)	0.5/0.25
D ₀ — D ₃	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
Q ₀ — Q ₃	Flip-flop Outputs	10/5.0
\bar{Q}_0 — \bar{Q}_3	Complement Outputs	(2.5) 10/5.0 (2.5)

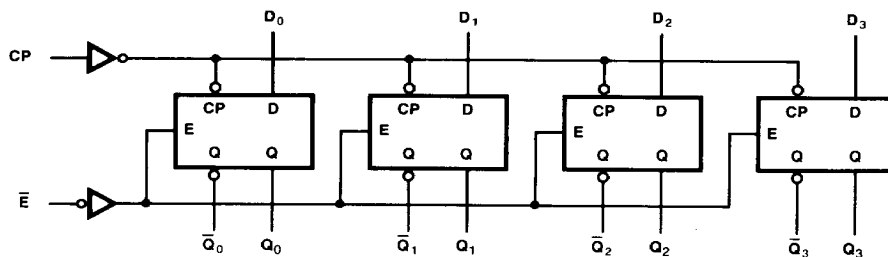
FUNCTIONAL DESCRIPTION — The '379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock (CP) and Enable (\bar{E}) inputs are common to all flip-flops. When the \bar{E} input is HIGH, the register will retain the present data independent of the CP input. The D_n and \bar{E} inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

TRUTH TABLE

INPUTS			OUTPUTS	
\bar{E}	CP	D_n	Q_n	\bar{Q}_n
H		X	No Change	No Change
L		H	H	L
L		L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I _{CC}	Power Supply Current		18	mA	V _{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C _L = 15 pF			
		Min	Max		
f _{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n		27 27	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t _s (H) t _s (L)	Setup Time HIGH or LOW D _n to CP	20		ns	Fig. 3-6
t _h (H) t _h (L)	Hold Time HIGH or LOW D _n to CP	5.0 5.0		ns	
t _s (H) t _s (L)	Setup Time HIGH or LOW E̅ to CP	25 25		ns	
t _h (H) t _h (L)	Hold Time HIGH or LOW E̅ to CP	5.0 5.0		ns	
t _w (L)	CP Pulse Width LOW	17		ns	Fig. 3-8

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