Signetics

74165
Shift Register

8-Bit Serial/Parallel-In, Serial-Out Shift Register
Product Specification

Logic Products

- **Asynchronous 8-bit parallel load**
- **Synchronous Serial input**
- **Clock Enable for "do nothing" mode**
- **See '166 for fully synchronous operation**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74165	26MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74165N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
$\overline{PL}$	Input	2ul
Other	Inputs	1ul
All	Outputs	10ul

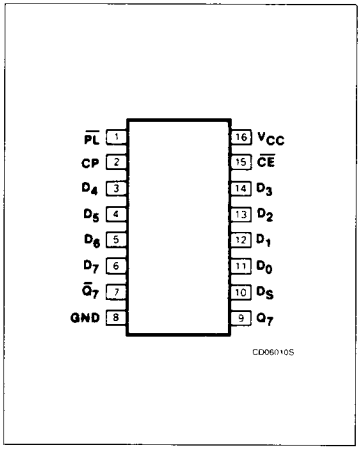
NOTE:
A 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

DESCRIPTION

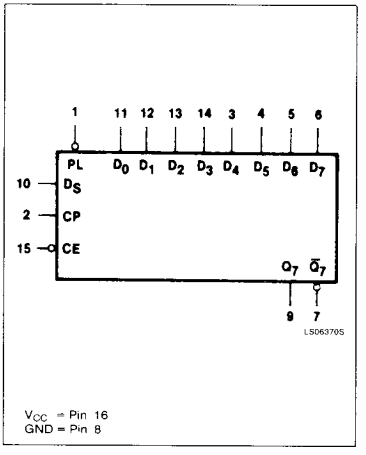
The '165 is an 8-bit parallel load or serial-in shift register with complementary Serial outputs (Q_7 and $\overline{Q}_7$) available from the last stage. When the Parallel Load ($\overline{PL}$) input is LOW, parallel data from the $D_0 - D_7$ inputs are loaded into the register asynchronously. When the $\overline{PL}$ input is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The Clock input is a gated-OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation. Also, the CP and $\overline{CE}$ inputs should be LOW before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is released.

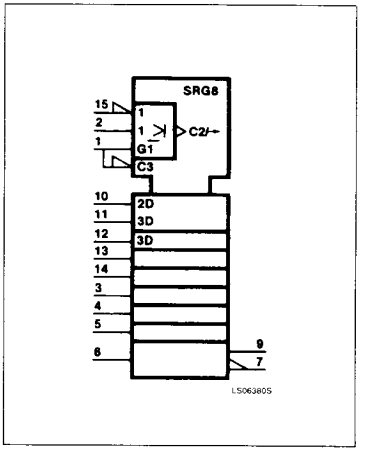
PIN CONFIGURATION



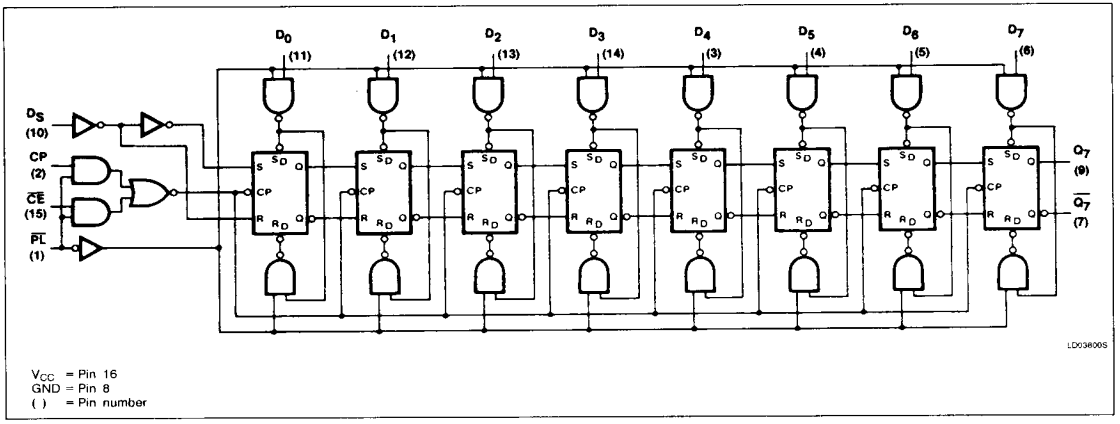
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_S	$D_0 - D_7$	Q_0	$Q_1 - Q_6$	Q_7	$\overline{Q}_7$
Parallel load	L	X	X	X	L	L	L – L	L	H
	L	X	X	X	H	H	H – H	H	L
Serial shift	H	L	↑	l	X	L	$q_0 - q_5$	q_6	$\overline{q}_6$
	H	L	↑	h	X	H	$q_0 - q_5$	q_6	$\overline{q}_6$
Hold "do nothing"	H	H	X	X	X	q_0	$q_1 - q_6$	q_7	$\overline{q}_7$

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−12	mA
I_{OH}	HIGH-level output current			−800	μA
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74165			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OL} = MAX			0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$\overline{PL}$ input			80	μA
			Other inputs			40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{PL}$ input			−3.2	mA
			Other inputs			−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−18		−55	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			42	63	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the outputs open, $\overline{CE}$ and CP at 4.5V, and a clock pulse applied to the $\overline{PL}$ input, I_{CC} is measured first with the Parallel Data inputs at 4.5V, then with the Parallel Data inputs grounded.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74		UNIT
			C_L = 15pF, R_L = 400Ω		
			Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		24 31	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to output	Waveform 2		31 40	ns
t_{PLH} t_{PHL}	Propagation delay D_7 to Q_7	Waveform 3		17 36	ns
t_{PLH} t_{PHL}	Propagation delay D_7 to $\overline{Q}_7$	Waveform 3		27 27	ns

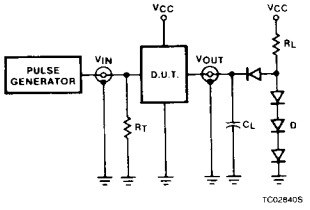
NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

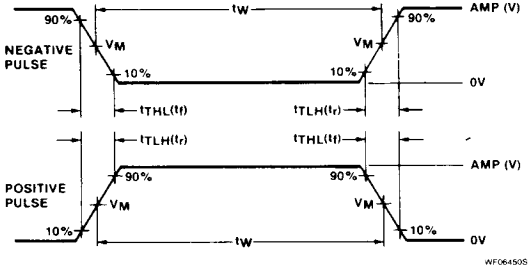
AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	25		ns
t_W	$\overline{PL}$ pulse width	Waveform 2	15		ns
t_S	Set-up time, D_S to clock	Waveform 4	20		ns
t_h	Hold time, D_S to clock	Waveform 4	0		ns
$t_S(L)$	Set-up time, LOW $\overline{CE}$ to clock	Waveform 4	30		ns
t_h	Hold time, $\overline{CE}$ to clock	Waveform 4	0		ns
t_S	$\overline{PL}$ set-up time to clock	Waveform 2	45		ns
t_S	Set-up time, D_5 and D_7 (1) to $\overline{PL}$	Waveform 5	10		ns

NOTE:
1. The remaining six Data inputs and D_S are LOW. Prior to test, HIGH level data is loaded into D_7 input.

TEST CIRCUITS AND WAVEFORMS





V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

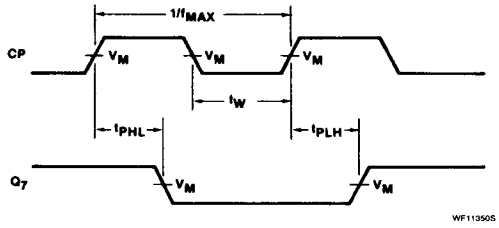
Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

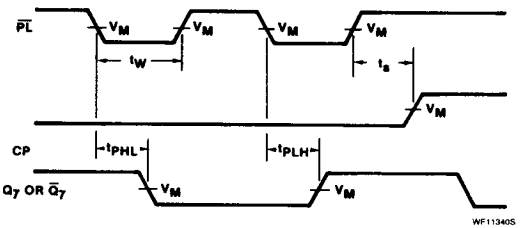
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

AC WAVEFORMS



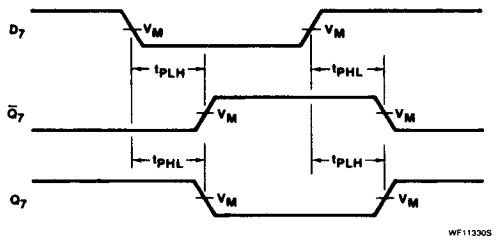
The changing output assumes internal Q_6 opposite site from Q_7.

Waveform 1. Clock To Output Delays And Clock Pulse Width



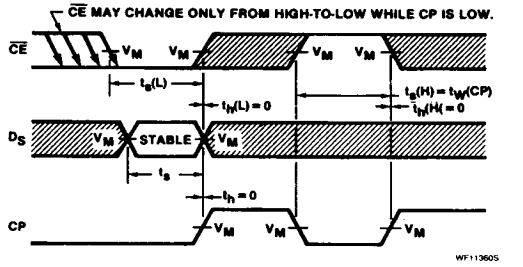
The changing output assumes internal Q_6 opposite site from Q_7.

Waveform 2. Parallel Load Pulse Width, $\overline{PL}$ To Output Delays And $\overline{PL}$ To Clock Set-up Time



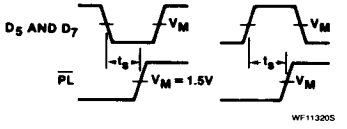
Conditions: $\overline{PL}$ = LOW

Waveform 3. Parallel Data To Output Delays



The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4. Clock Enable And Serial Data Set-up And Hold Times



For all waveforms, V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 5. Set-up Times To Active Low Parallel Load