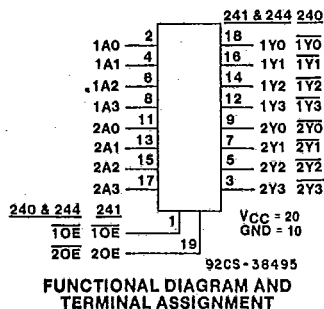


**CD54/74HC240/241/244**  
**CD54/74HCT240/241/244**

File Number 1656

**High-Speed CMOS Logic**

HARRIS SEMICONDUCTOR 27E D ■ 4302271 0017705 7 ■ HAS



**Octal Buffer/Line Drivers, 3-State**

CD54/74HC/HCT240 Inverting  
CD54/74HC/HCT241 Non-Inverting  
CD54/74HC/HCT244 Non-Inverting

**Type Features:**

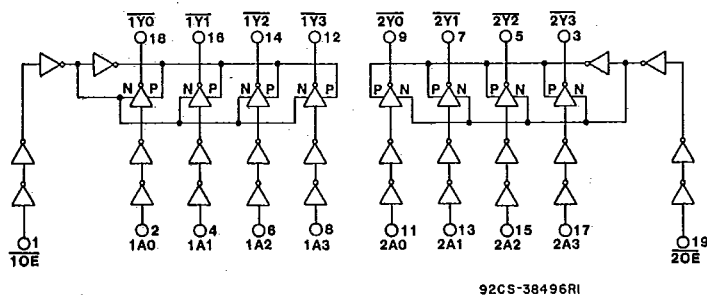
- Typical propagation delay = 8 ns @  $V_{CC}=5V, C_L=15pF, T_A=25^\circ C$  for HC240
- 3-State outputs
- Buffered inputs
- High-current bus driver outputs

The RCA-CD54/74HC240 and CD54/74HCT240 are inverting 3-state buffers having two active-low output enables. The RCA CD54/74HC/HCT241 and CD54/74HC/HCT244 are non-inverting 3-state buffers that differ only in that the 241 has one active-high and one active-low output enable, and the 244 has two active-low output enables. All three types have identical pinouts.

The CD54HC240/241/244 and CD54HCT240/241/244 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC240/241/244 and CD74HCT240/241/244 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT240/241/244 are also supplied in chip form (H suffix).

**Family Features:**

- Fanout (Over Temperature Range):  
Standard Outputs - 10 LSTTL Loads  
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:  
CD74HC/HCT:  $-40$  to  $+85^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:  
2 to 6 V Operation  
High Noise Immunity:  
 $N_{IL}=30\%, N_{IH}=30\%$  of  $V_{CC}$ : @  $V_{CC}=5V$
- CD 54HCT/CD74HCT Types:  
4.5 to 5.5 V Operation  
Direct LSTTL Input Logic Compatibility  
 $V_{IL}=0.8V$  Max.,  $V_{IH}=2V$  Min.  
CMOS Input Compatibility  
 $I_I \leq 1\mu A$  @  $V_{OL}, V_{OH}$



**TRUTH TABLE**

INPUTS		OUTPUT
$\overline{1OE}, \overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

(HC/HCT240)

Fig. 1 - CD54/74HC/HCT240 logic diagram.

CD54/74HC240/241/244  
CD54/74HCT240/241/244

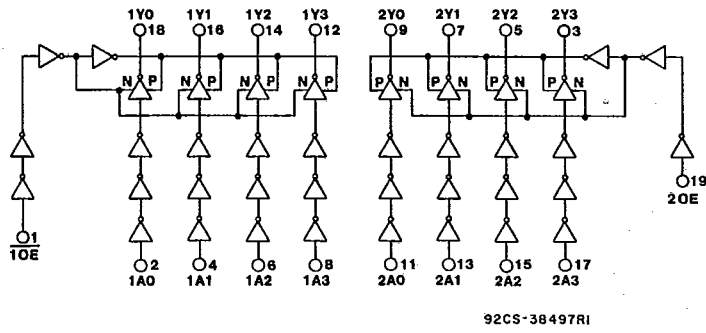


Fig. 2 - CD54/74HC/HCT241 logic diagram.

TRUTH TABLE

INPUTS		OUTPUT	INPUTS		OUTPUT
1OE	1A	1Y	2OE	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

H=HIGH Voltage Level (HCT/HCT241)  
L=LOW Voltage Level  
X=Immaterial  
Z=HIGH Impedance

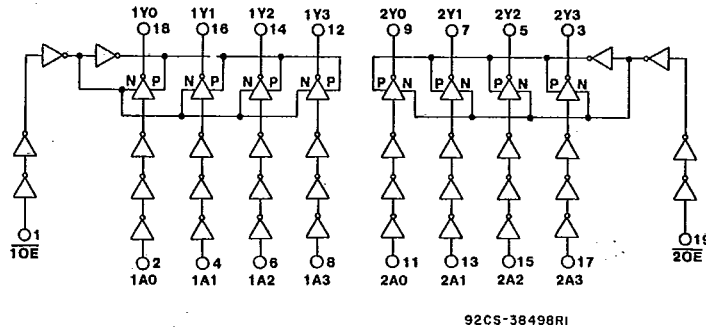


Fig. 3 - CD54/74HC/HCT244 logic diagram.

TRUTH TABLE

INPUTS		OUTPUT	
1OE, 2OE	A	Y	
L	L	L	L
L	H	H	H
H	X	X	Z

(HC/HCT244)

**CD54/74HC240/241/244**  
**CD54/74HCT240/241/244**

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE, (V<sub>cc</sub>):  
 (Voltages referenced to ground) ..... -0.5 to +7 V

DC INPUT DIODE CURRENT, I<sub>IK</sub> (FOR V<sub>i</sub> < -0.5 V OR V<sub>i</sub> > V<sub>cc</sub> +0.5 V) ..... ±20 mA

DC OUTPUT DIODE CURRENT, I<sub>OK</sub> (FOR V<sub>o</sub> < -0.5 V OR V<sub>o</sub> > V<sub>cc</sub> +0.5 V) ..... ±20 mA

DC DRAIN CURRENT, PER OUTPUT (I<sub>o</sub>) (FOR -0.5 V < V<sub>o</sub> < V<sub>cc</sub> +0.5 V) ..... ±35 mA

DC V<sub>cc</sub> OR GROUND CURRENT, (I<sub>cc</sub>) ..... ±70 mA

POWER DISSIPATION PER PACKAGE (P<sub>o</sub>):

For T<sub>A</sub> = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW

For T<sub>A</sub> = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW

For T<sub>A</sub> = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW

For T<sub>A</sub> = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW

For T<sub>A</sub> = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW

For T<sub>A</sub> = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>):

PACKAGE TYPE F, H ..... -55 to +125°C

PACKAGE TYPE E, M ..... -40 to +85°C

STORAGE TEMPERATURE (T<sub>stg</sub>) ..... -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only ..... +300°C

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T <sub>A</sub> =Full Package-Temperature Range) V <sub>cc</sub> .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V <sub>i</sub> , V <sub>o</sub>	0	V <sub>cc</sub>	V
Operating Temperature T <sub>A</sub> :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t <sub>r</sub> , t <sub>f</sub>			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

\*Unless otherwise specified, all voltages are referenced to Ground.

HARRIS SEMICONDUCTOR  
 27E D  
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CD54/74HC240/241/244  
CD54/74HCT240/241/244

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC240/241/244, CD54HC240/241/244										CD74HCT240/241/244, CD54HCT240/241/244										UNITS
	TEST CONDITIONS		V <sub>CC</sub> V	74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		V <sub>CC</sub> V	74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V <sub>I</sub> V	I <sub>O</sub> mA		+25°C			-40/ +85°C		-55/ +125°C		V <sub>I</sub> V	V <sub>CC</sub> V		+25°C			-40/ +85°C		-55/ +125°C		
			Min	Typ	Max	Min	Max	Min	Max	Min			Typ	Max	Min	Max	Min	Max			
High-Level Input Voltage V <sub>IH</sub>			2	1.5	—	—	1.5	—	1.5	—	—	4.5									V
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—		
			6	4.2	—	—	4.2	—	4.2	—	—	5.5									
Low-Level Input Voltage V <sub>IL</sub>			2	—	—	0.5	—	0.5	—	0.5	—	4.5									V
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	—	
			6	—	—	1.8	—	1.8	—	1.8	—	5.5									
High-Level Output Voltage V <sub>OH</sub> CMOS Loads	V <sub>IL</sub> or V <sub>IH</sub>	-0.02	2	1.9	—	—	1.9	—	1.9	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	3.98	—	—	3.84	—	3.7	—		
			6	5.9	—	—	5.9	—	5.9	—	V <sub>IH</sub>	4.5	3.98	—	—	3.84	—	3.7	—		
Low-Level Output Voltage V <sub>OL</sub> CMOS Loads	V <sub>IL</sub> or V <sub>IH</sub>	0.02	2	—	—	0.1	—	0.1	—	0.1	V <sub>IL</sub> or V <sub>IH</sub>	4.5	—	—	0.1	—	0.1	—	0.1	—	V
			4.5	—	—	0.1	—	0.1	—	0.1	or	4.5	—	—	0.26	—	0.33	—	0.4		
			6	—	—	0.1	—	0.1	—	0.1	V <sub>IH</sub>	4.5	—	—	0.26	—	0.33	—	0.4		
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage between V <sub>CC</sub> & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
			6	—	—	±0.1	—	±1	—	±1	or	5.5	—	—	±0.1	—	±1	—	±1		
			6	—	—	±0.1	—	±1	—	±1	Gnd	5.5	—	—	±0.1	—	±1	—	±1		
Quiescent Device Current I <sub>CC</sub>	V <sub>CC</sub> or Gnd	0	6	—	—	8	—	80	—	160	V <sub>CC</sub> or Gnd	5.5	—	—	8	—	80	—	160		μA
			6	—	—	8	—	80	—	160	or	5.5	—	—	8	—	80	—	160		
			6	—	—	8	—	80	—	160	Gnd	5.5	—	—	8	—	80	—	160		
Additional Quiescent Device Current per Input pin: 1 unit load ΔI <sub>CC</sub> *											V <sub>CC</sub> -2.1 4.5 to 5.5	—	100	360	—	450	—	490		μA	
3-state leakage current I <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> =V <sub>CC</sub> or Gnd	6	—	—	±0.5	—	±5	—	±10	V <sub>IL</sub> or V <sub>IH</sub>	5.5	—	—	±0.5	—	±5	—	±10		μA

\*For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

**CD54/74HC240/241/244**  
**CD54/74HCT240/241/244**

HCT Input Loading Tables

CD54/74HCT240	
Input	Unit Loads*
nA0-A3	1.5
1OE	0.7
2OE	0.7

CD54/74HCT241	
Input	Unit Loads*
nA0-A3	0.7
1OE	0.7
2OE	1.5

CD54/74HCT244	
Input	Unit Loads*
nA0-A3	0.7
1OE	0.7
2OE	0.7

\*Unit Load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 360  $\mu$ A max. @ 25°C.

**SWITCHING CHARACTERISTICS (V<sub>CC</sub>=5 V, T<sub>A</sub>=25°C, Input t<sub>r</sub>=6 ns)**

CHARACTERISTIC	SYMBOL	C <sub>L</sub> pF	Typical Values						UNITS
			240		241		244		
			HC	HCT	HC	HCT	HC	HCT	
Propagation Delay Data to Output	t <sub>PHL</sub> t <sub>PLH</sub>	15	8	9	9	10	9	10	ns
Output Disable/Enable to Outputs	t <sub>PZH</sub> , t <sub>PZL</sub> , t <sub>PHZ</sub> , t <sub>PLZ</sub>	15	12	12	12	12	12	12	ns
Power Dissipation Capacitance	C <sub>PD</sub> *	—	38	40	34	38	46	40	pF

C<sub>PD</sub> is used to determine the dynamic power consumption per channel.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

f<sub>i</sub> = input frequency.

C<sub>L</sub> = output load capacitance.

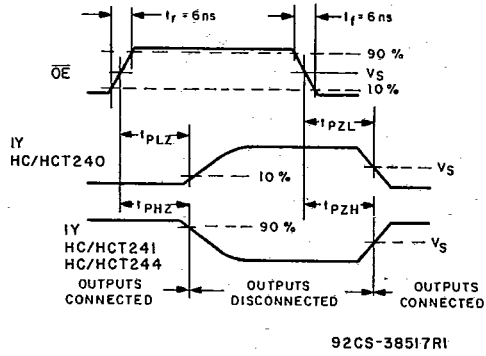
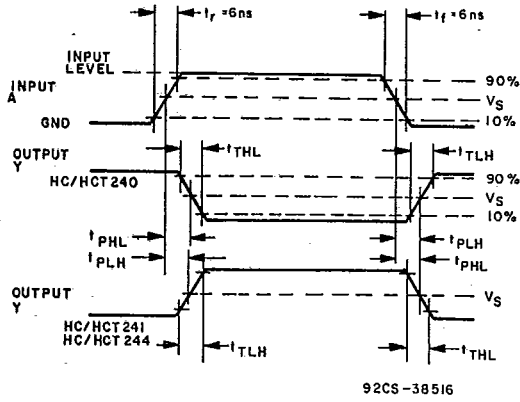
V<sub>CC</sub> = supply voltage.

**SWITCHING CHARACTERISTICS (C<sub>L</sub>=50 pF, Input t<sub>r</sub>=6 ns)**

CHARACTERISTIC	SYMBOL	V <sub>CC</sub>	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Data to Outputs	t <sub>PLH</sub>	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
HC/HCT 240	t <sub>PHL</sub>	4.5	—	20	—	22	—	25	—	28	—	30	—	33	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Data to Outputs	t <sub>PLH</sub>	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
HC/HCT 241	t <sub>PHL</sub>	4.5	—	22	—	25	—	28	—	31	—	33	—	38	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Data to Outputs	t <sub>PLH</sub>	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
HC/HCT 244	t <sub>PHL</sub>	4.5	—	22	—	25	—	28	—	31	—	33	—	38	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Output Enable and Disable Times	t <sub>PZH</sub> t <sub>PZL</sub> t <sub>PHZ</sub> t <sub>PLZ</sub>	2 4.5 6	— — —	150 30 26	— — —	— 30 —	— — —	190 38 33	— — —	— 38 —	— — —	225 45 38	— — —	— 45 —	ns
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>	2 4.5 6	— — —	60 12 10	— — —	— 12 —	— — —	75 15 13	— — —	— 15 —	— — —	90 18 15	— — —	— 18 —	ns
Input Capacitance	C <sub>i</sub>		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C <sub>o</sub>		—	20	—	20	—	20	—	20	—	20	—	20	pF

HAS 4 0017709 4302271 27E D HARRIS SEMICONDUCTOR SECTOR

T-52-09 Technical Data  
**CD54/74HC240/241/244**  
**CD54/74HCT240/241/244**



	54/74HC	54/74HCT
Input Level	VCC	3 V
Switching Voltage, Vs	50% VCC	1.3 V

Fig. 2 - Transition times and propagation delay times.

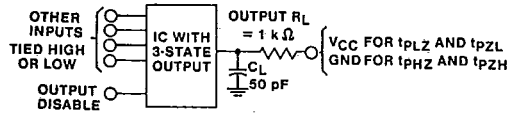


Fig. 4 - Three-state propagation delay test circuit.