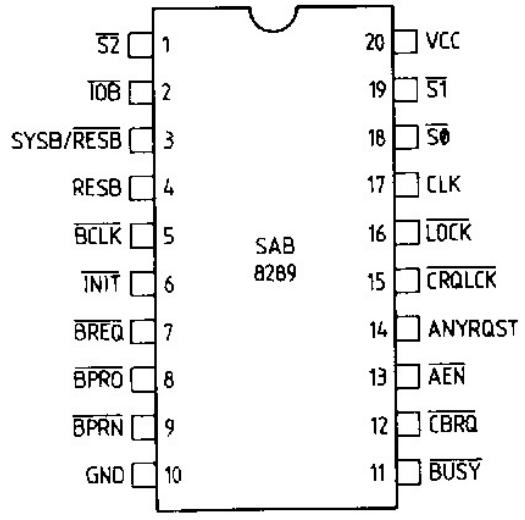
Preliminary

SAB 8289
Bus Arbiter

SAB 8289 8 MHz
SAB 8289-1 10 MHz

- Provides Multi-Master System Bus Protocol
- Synchronizes SAB 8086/SAB 8088 Processors with Multi-Master Bus
- Provides Simple Interface with SAB 8288 Bus Controller
- Four Operating Modes for Flexible System Configuration
- Compatible with Intel Bus Standard MULTIBUS™ (MULTIBUS is a trademark of INTEL Corporation USA)
- Provides System Bus Arbitration for SAB 8089 IOP in Remote Mode

Pin Configuration



Pin Names

$\overline{S0}$-2	Status
$\overline{IOB}$	I/O Bus Present
SYSB/$\overline{RESB}$	System/Resident Bus
RESB	Resident Bus Present
$\overline{BCLK}$	Bus Clock
$\overline{INIT}$	Initialisation
$\overline{BREQ}$	Bus Request
$\overline{BPRO}$	Bus Priority Out
$\overline{BPRN}$	Bus Priority In
CLK	System Clock
$\overline{AEN}$	Address Enable
ANYRQST	Any Request
$\overline{CRQLCK}$	Common Request Lock
$\overline{CBRQ}$	Common Bus Request
$\overline{LOCK}$	Bus Lock
VCC	+5 V
GND	Ground (0V)

The SAB 8289 Bus Arbiter is a 20-pin, 5-volt-only bipolar component for use with medium to large SAB 8086/SAB 8088 multi-master/multiprocessing systems. The SAB 8289 provides system bus arbitration for systems with multiple bus masters, such as an SAB 8086 CPU with SAB 8089 IOP in its REMOTE mode, while providing bipolar buffering and drive capability.

Pin Definitions and Functions

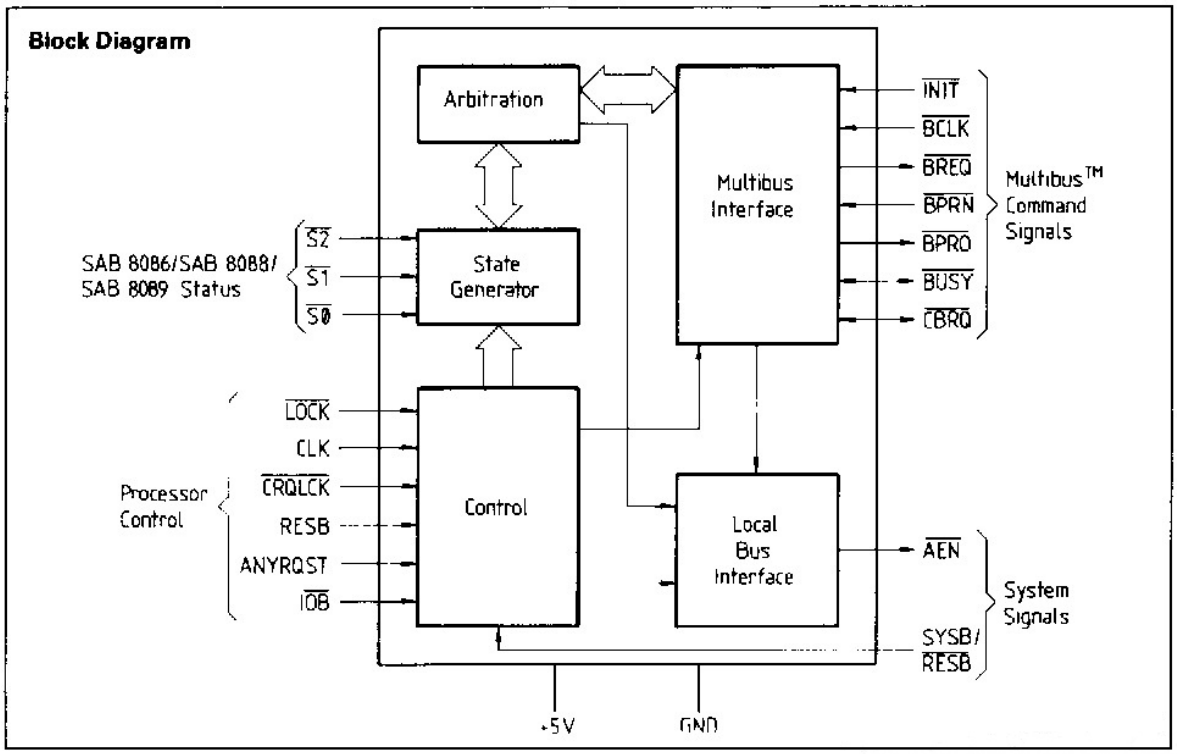
Symbol	Number	Input (I) Output (O)	Function
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	1, 18, 19	I	**Status Input Pins** These pins are the status input pins from a SAB 8086, SAB 8088 or SAB 8089 processor. The SAB 8289 decodes these pins to initiate bus request and surrender actions.
CLK	17	I	**Clock** This is the clock from the SAB 8284A clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	16	I	**Lock** $\overline{LOCK}$ is a processor generated signal which when activated (low) serves to prevent the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	15	I	**Common Request Lock** $\overline{CRQLCK}$ is an active low signal which serves to prevent the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	4	I	**Resident Bus** RESB is a strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. When it is strapped high the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. When it is strapped low the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	14	I	**Any Request** ANYRQST is a strapping option which permits the multimaster system bus to be surrendered to a lower priority arbiter as though it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). Strapping $\overline{CBRQ}$ low and ANYRQST high forces the SAB 8289 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs $\overline{BREQ}$ is driven false (high).
$\overline{IOB}$	2	I	**IO Bus** $\overline{IOB}$ is a strapping option which configures the SAB 8289 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multimaster system bus. The arbiter requests and surrenders the use of the multimaster system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as would be an IO command.
$\overline{AEN}$	13	O	**Address Enable** $\overline{AEN}$ is the output of the SAB 8289 Arbiter to the processor's address latches, to the SAB 8288 Bus Controller and SAB 8284A Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to tri-state their output drivers.

Symbol	Number	Input (I) Output (O)	Function
SYSB/$\overline{\text{RESB}}$	3	I	**System Bus/Resident Bus** SYSB/$\overline{\text{RESB}}$ is an input signal when the arbiter is configured in the S.R. Mode (RESB is strapped high) which serves to determine when the multimaster system bus is requested and when the multi-master system bus surrendering is permitted. The signal is intended to originate from some form of address mapping circuitry such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from Ø1 of T4 to Ø1 to T2 of the processor cycle. During the period from Ø1 of T2 to Ø1 of T4 only clean transitions are permitted on this pin (no glitches). If a glitch does occur the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the S.R. Mode when the state of the SYSB/$\overline{\text{RESB}}$ pin is high and permits the bus to be surrendered when this pin is low.
$\overline{\text{CBRQ}}$	12	I/O	**Common Bus Request** $\overline{\text{CBRQ}}$ is an input signal which serves to instruct the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{\text{CBRQ}}$ pins (open-collector output) of all the SAB 8289 Bus Arbiters which are to surrender the multi-master-system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{\text{CBRQ}}$ line low. Any other arbiter connected to the $\overline{\text{CBRQ}}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{\text{BREQ}}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{\text{CBREQ}}$ low and ANYRQST – high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{\text{INIT}}$	6	I	**Initialize** $\overline{\text{INIT}}$ is an active low multimaster system bus input signal which is used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
$\overline{\text{BCLK}}$	5	I	**Bus Clock** $\overline{\text{BCLK}}$ is the multi-master system bus clock to which all multimaster system bus interface signals are synchronized.
$\overline{\text{BREQ}}$	7	O	**Bus Request** $\overline{\text{BREQ}}$ is an active low output signal in the parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{\text{BPRN}}$	9	I	**Bus Priority In** $\overline{\text{BPRN}}$ is the active low signal returned to the arbiter to instruct it that it may acquire the multimaster system bus on the next falling edge of BCLK. $\overline{\text{BPRN}}$ indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{\text{BPRN}}$ instructs the arbiter that it has loss priority to a higher priority arbiter

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{BPRO}$	8	O	**Bus Priority Out** $\overline{BPRO}$ is an active low output signal which is used in the serial priority resolving scheme where $\overline{BPRO}$ is daisy chained to $\overline{BPRN}$ of the next lower priority arbiter.
$\overline{BUSY}$	11	I/O	**Busy** $\overline{BUSY}$ is an active low open collector multi-master system bus interface signal which is used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{BPRN}$) seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus it releases the $\overline{BUSY}$ signal permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.
VCC	20	I	**Power Supply** (+5 V ± 10%)
GND	10	I	**Ground** (0V)

Block Diagram



Functional Description

The SAB 8289 Bus Arbiter operates in conjunction with the SAB 8288 Bus Controller to interface SAB 8086/SAB 8088/ SAB 8089 processors to a multi-master system bus (both the SAB 8086 and the SAB 8088 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (SAB 8288), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the SAB 8288, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

Arbitration between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multimaster system bus is surrendered or requested under different sets of conditions.

Modes of Operation

There are two types of processors in the SAB 8086 family. An Input/Output processor (the SAB 8089 IOP) and the SAB 8086/SAB 8088 CPUs. Consequently, there are two basic operating modes in the SAB 8289 bus arbiter. One, the $\overline{\text{IOB}}$ (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{\text{IOB}}$ strapping option configures the SAB 8289 Bus Arbiter into the $\overline{\text{IOB}}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only. With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{\text{IOB}}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus.

The SAB 8086 and SAB 8088 processor can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration. In such a system configuration the processor would have access to memory and peripheral of both busses. Memory mapping techniques are applied to select which bus is to be accessed. The SYSB/$\overline{\text{RESB}}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{\text{RESB}}$ also enables or disables commands from one of the bus controllers.

Summary of SAB 8289 Modes, Requesting and Relinquisting the Multi-master system bus

	Status Lines From SAB 8086 / 88 / 89			IOB Mode Only	RESB (Mode) Only IOB=High RESB=High		IOB Mode RESB Mode IOB=Low RESB=High		Single Bus Mode IOB=High RESB=Low
	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	IOB=Low	SYSB/$\overline{RESB}$ =High	SYSB/$\overline{RESB}$ =Low	SYSB/$\overline{RESB}$ =High	SYSB/$\overline{RESB}$ =Low	
I/O	0	0	0	x		x	x	x	
COMMANDS	0	0	1	x		x	x	x	
	0	1	0	x		x	x	x	
HALT	0	1	1	x	x	x	x	x	x
MEM	1	0	0			x		x	
COMMANDS	1	0	1			x		x	
	1	1	0			x		x	
IDLE	1	1	1	x	x	x	x	x	x

NOTE:
x = Multi-Master System Bus is allowed to be Surrendered.

Mode	Pin Strapping	Multi-Master System Bus	
		Requested**	Surrendered*
Single Bus Multi-Master Mode	$\overline{IOB}$=High RESB=Low	Whenever the processor's status lines go active	HLT+TI•CBRQ+HPBRQ***
RESB Mode Only	$\overline{IOB}$=High RESB=High	SYSB/$\overline{RESB}$=High• ACTIVE STATUS	(SYSB/$\overline{RESB}$=Low+TI)• CRBQ+HLT+HPBRQ
IOB Mode Only	IOB=Low RESB=Low	Memory Commands	(I/O Status+TI)•CBRQ+ HLT+HPBRQ
IOB Mode•RESB Mode	$\overline{IOB}$=Low RESB=High	(Memory Command)• (SYSB/$\overline{RESB}$=High)	((I/O Status Commands)+ SYSB/RESB=LOW))•CBRQ +HPBRQ***+HLT

NOTES:
*$\overline{LOCK}$ prevents surrender of Bus to any other arbiter, $\overline{CRQLCK}$ prevents surrender of Bus to any lower priority arbiter.
**Except for HALT and Passive or IDLE Status.
***HPBRQ, Higher priority Bus request or $\overline{BPRN}$ = 1.
1. $\overline{IOB}$ Active Low.
2. RESB Active High.
3. + is read as "OR" and• as "AND".
4. TI=Processor Idle Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$=111
5. HLT=Processor Halt Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$=011

Absolute Maximum Ratings*

Ambient Temperature Under Bias 0 to 70°C
Storage Temperature –65 to 150°C
All Output and Supply Voltages –0.5 to 7 V
All Input Voltages –1.0 to 5.5 V
Power Dissipation 1.5 Watt

D.C. Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 10%

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
V_C	Input Clamp Voltage	–	–1.0	V	V_{CC}=4.5 V, I_C=–5 mA
I_F	Input Forward Current	–	–0.5	mA	V_{CC}=5.5 V, V_F=0.45 V
I_R	Reverse Input Leakage Current	–	60	µA	V_{CC}=5.5 V, V_R=5.5 V
V_{OL}	Output Low Voltage $\overline{BUSY}$, $\overline{CBRQ}$ $\overline{AEN}$ $\overline{BPRO}$, $\overline{BREQ}$	–	0.45	V	I_{OL}=20 mA I_{OL}=16 mA I_{OL}=10 mA
V_{OH}	Output High Voltage $\overline{BUSY}$, $\overline{CBRQ}$	Open Collector			–
	All Other Outputs	2.4	–	V	I_{OH}=400 µA
I_{CC}	Power Supply Current	–	165	mA	–
V_{IL}	Input Low Voltage	–	0.8	V	
V_{IH}	Input High Voltage	2.0	–		
C_{in} Status	Input Capacitance	–	25	pF	
C_{in} (Others)	Input Capacitance	–	12		

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended perods may affect device reliability.

A.C. Characteristics

T_A=0 to 70°C, V_{CC}=5 V ± 10%

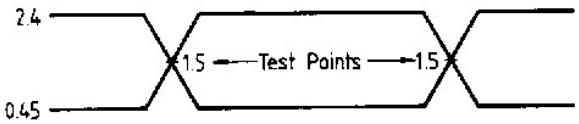
Timing Requirements

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8289		SAB 8289-1			
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	125	–	100	–	ns	–
TCLCH	CLK Low Time	65		53			
TCHCL	CLK High Time	35		35			
TSVCH	Status Active-Setup	65	TCLCL-10	55	TCLCL-10		
TSHCL	Status Inactive-Setup	50		45			
THVCH	Status Active Hold	10	–	10	–		
THVCL	Status Inactive Hold						
TBYSBL	Busy↑↓Setup to BCLK↓	20		20			
TCBSBL	CBRQ↑↓Setup to BCLK↓						
TBLBL	BCLK Cycle Time	100		100			
TBHCL	BCLK High Time	30	0.65 [TBLBL]	30	0.65 [TBLBL]		
TCLLL1	LOCK Inactive Hold	10	–	10	–		
TCLLL2	LOCK Active Setup	40		40			
TPNBL	BPRN↓↑ to BCLK Setup Time	15		15			
TCLSR1	SYSB/RESB Setup	0		0			
TCLSR2	SYSB/RESB Hold	20		20			
TNIH	Initialization Pulse Width	3TBLBL+ 3TCLCL		3TBLBL+ 3TCLCL			
TILIH	Input Rise Time	–	20	–	20		From 0.8 to 2.0 V
TIHIL	Input Fall Time		12		12		From 2.0 to 0.8 V

↑↓ Denotes the spec applies to both transitions of the signal.

A.C. Testing Input/Output Waveform

Input/Output



A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". The clock is driven at 4.3 V and 0.25 V. Timing measurements are made at 1.5 V for both a logic "1" and "0".

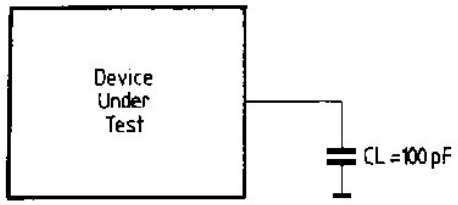
Timing Responses

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
TBLBRL	BCLK to BREQ Delay↓↑	–	35	–	–
TBLPOH	BCLK to BPRO↓↑[1]		40		
TPNPO	BPRN↓↑ to BPRO↓↑ Delay[1]		25		
TBLBYL	BCLK to BUSY Low		60		
TBLBYH	BCLK to BUSY Float[2]		35		
TCLAEH	CLK to AEN High		65	ns	
TBLAEL	BCLK to AEN Low		40		
TBLCBL	BCLK to CBRQ Low		60		
TBLCRH	BCLK to CBRQ Float[2]		35		
TOLOH	Output Rise Time		20		From 0.8 to 2.0 V
TOHOL	Output Fall Time		12		From 2.0 to 0.8 V

↓↑ Denotes the spec applies to both transitions of the signal.

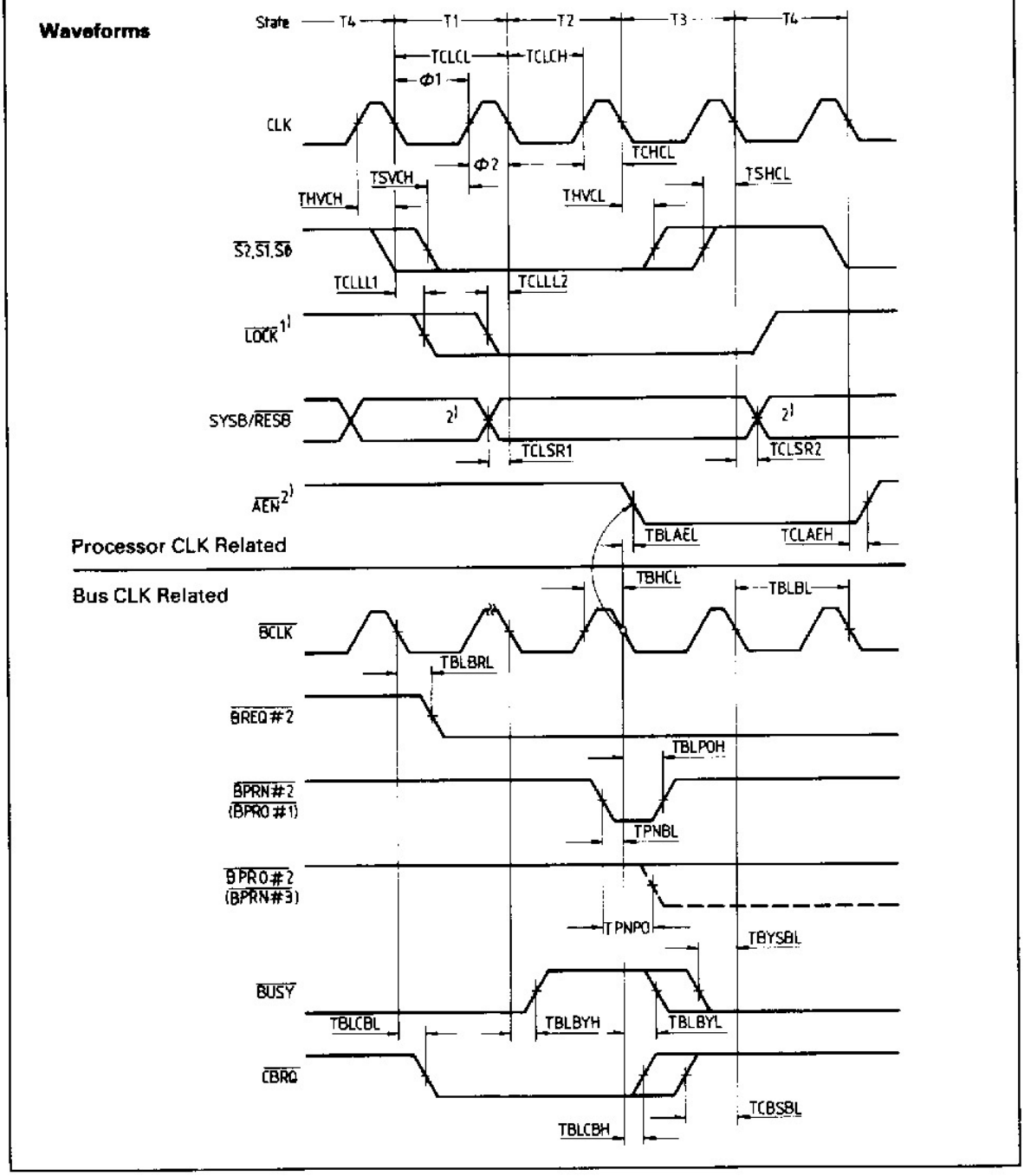
NOTES:
[1] BCLK generates the first BPRO wherein subsequent BPRO changes lower in the chain are generated through BPRON.
[2] Measured at 0.5 V above GND.

A.C. Testing Load Circuit



C_L = 100 pF
C_L Includes jig capacitance

Waveforms



NOTES:

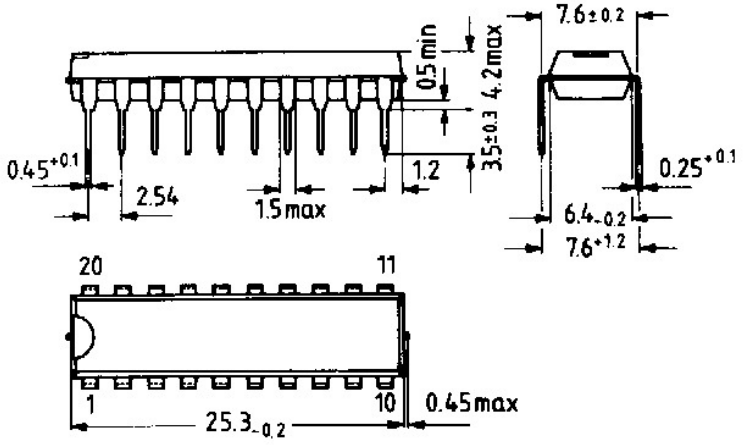
1. LOCK active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained.
   LOCK inactive has not critical time and can be asynchronous.
   CROLCK has no critical timing and is considered an asynchronous input signal.
2. Glitching of SYSB/RESB pin is permitted during this time. After I 2 of T1, and before I 1 of T4, SYSB/RESB should be stable.
3. AEN leading edge is related to BCLK, trailing edge to CLK. The trailing edge of AEN occurs after bus priority is lost.

Additional Notes:
The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to $\overline{BCLK}$. The signals shown related to the $\overline{BCLK}$ represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme as shown in Figure 6. Assume arbiter has the bus and is holding busy low. Arbiter #2 detects its processor wants the bus and pulls low $\overline{BREQ}$#2. If $\overline{BPRN}$#2 is high (as shown), arbiter #2 will pull low $\overline{CBRQ}$ line. $\overline{CBRQ}$ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{CBRQ}$].** Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Table 1), by lowering its $\overline{BPRO}$#1 (tied to $\overline{BPRN}$#2) and releasing BUSY. Arbiter #2 now sees that it has priority from $\overline{BPRN}$#2 being low and releases CBRQ. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its $\overline{BPRO}$#2 [TPNPO].

**Note that even a higher priority arbiter which is acquiring the bus through $\overline{BPRN}$ will momentarily drop $\overline{CBRQ}$ until it has acquired the bus.

Package Outline

20 Pin Plastic Package-Type P



Ordering Information

Component	Description	Ordering Code
SAB 8289-P	Bus-Arbiter 8 MHz (plastic)	Q67020-Y74
SAB 8289-1-P	Bus-Arbiter 10 MHz (plastic)	Q67120-Y85