

# TA7739P/F

## 3V DUAL PREAMPLIFIER.

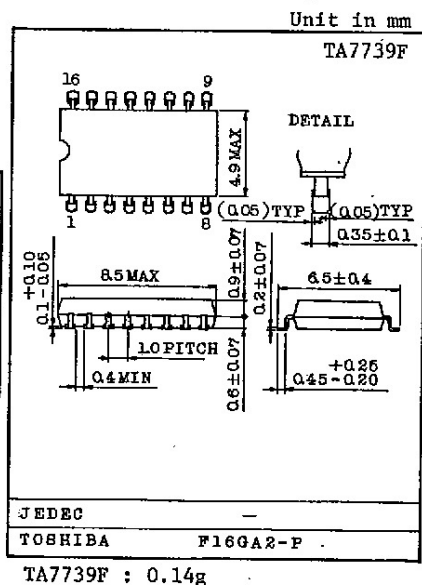
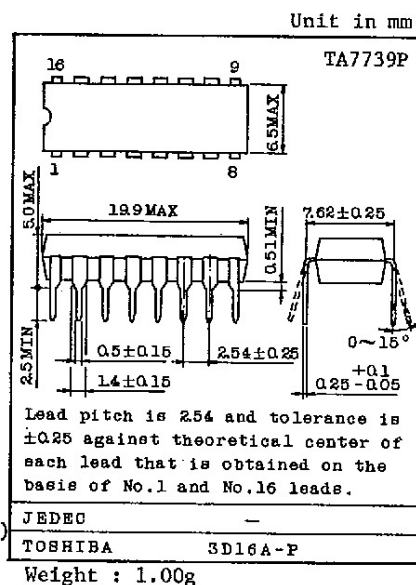
The TA7739P(DIP-16) and TA7739F(MFP-16-SO) are dual preamplifier designed for a 3V operation automatic reverse type headphone stereo application.

- . Built-in Forward/Reverse Control Switch
- . Built-in Metal/Normal Control Switch
- . No Input Coupling Capacitor
- . Low Noise :  $V_{NI}=0.9\mu V_{rms}(Typ.)$   
( $R_g=2.2k\Omega$ ,  $NAB(G_v=40dB, f=1kHz)$ )
- . Low Supply Current  
:  $I_{CCQ}=1.8mA(Typ.)$  ( $V_{CC}=3V, V_{IN}=0V$ )
- . High Output Voltage  
:  $V_{OM}=0.9V_{rms}(Typ.)$  ( $THD=0.5\%, V_{CC}=3V$ )
- . Wide Operating Supply Voltage :  $V_{CC}=1.6V-5V$  ( $T_a=25^\circ C$ )

### MAXIMUM RATINGS ( $T_a=25^\circ C$ )

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	6	V
Power Dissipation (Note)	TA7739P	$P_{D1}$	750
	TA7739F	$P_{D2}$	350
Operating Temperature	$T_{opr}$	-25~75	$^\circ C$
Storage Temperature	$T_{stg}$	-55~150	$^\circ C$

Note: Derated above  $T_a=25^\circ C$  in the proportion of  $6mW/^\circ C$  for TA7739P and of  $2.8mW/^\circ C$  for TA7739F.



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## ELECTRICAL CHARACTERISTICS

(Unless otherwise specified,  $V_{CC}=3V$ ,  $f=1kHz$ ,  $T_a=25^\circ C$ , NAB-Circuit)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	ICCQ	-	$V_{IN}=0V$	-	1.8	2.4	mA
Open Loop Voltage Gain	GVO	-		-	80	-	dB
Maximum Output Voltage	VOM	-	THD=0.5%	0.75	0.90	-	V <sub>rms</sub>
Total Harmonic Distortion	THD	-	$V_O=0.32V_{rms}$	-	0.025	0.1	%
Equivalent Input Noise Voltage	VNI	-	$R_g=2.2k\Omega$ , BW=30Hz~20kHz NAB (Gv=40dB)	-	0.9	1.7	$\mu V_{rms}$
Cross Talk F/R	C.T(F/R)	-	$V_O=0.32V_{rms}$ , $R_g=2.2k\Omega$	55	65	-	dB
Cross Talk CH1/CH2	C.T	-	$V_O=0.32V_{rms}$ , $R_g=2.2k\Omega$	55	65	-	dB
Ripple Rejection	R.R	-	$f=100Hz$ , $V_R=0.32V_{rms}$	-	45	-	dB

## TYPICAL DC VOLTAGE OF EACH TERMINAL

( $V_{CC}=3V$ ,  $T_a=25^\circ C$ ,  $V_{IN}=0V$ , by Test Circuit)

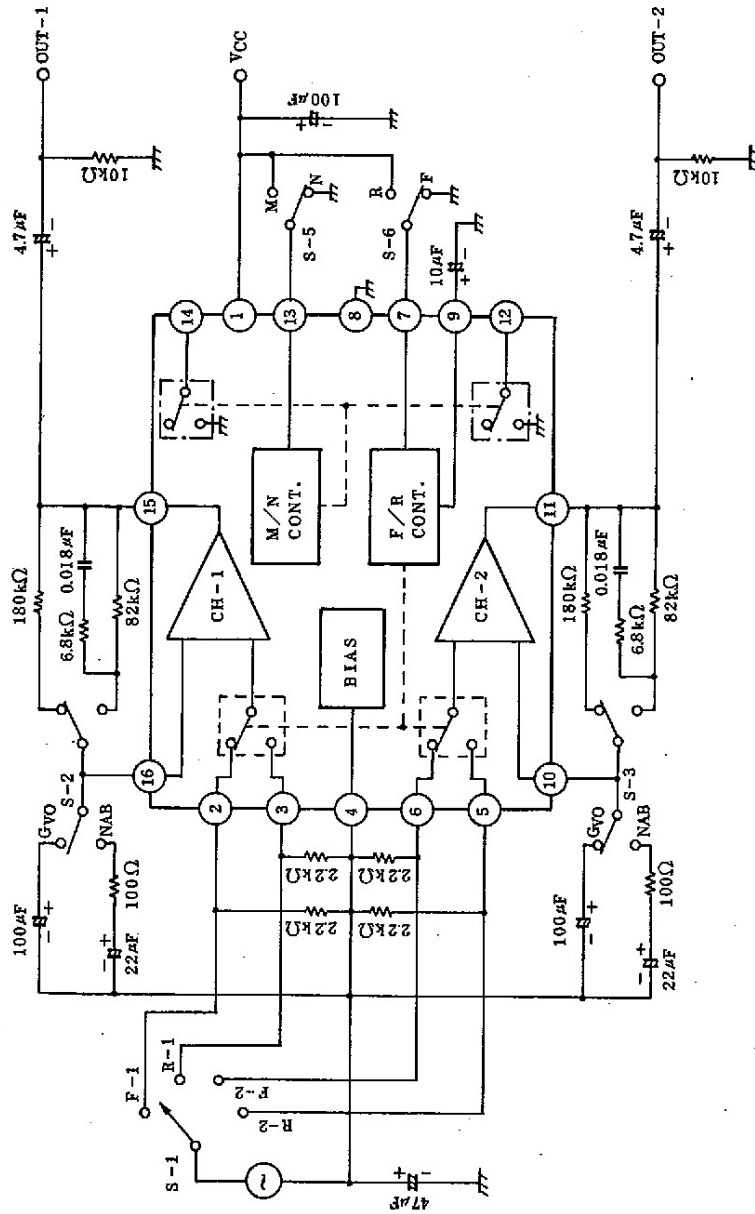
TERMINAL No.	1	2	3	4	5	6	7	8
DC-Voltage (V)	3	1.50	1.50	1.50	1.50	1.50	3.0/0	0

TERMINAL No.	9	10	11	12	13	14	15	16
DC-Voltage (V)	0.90	1.50	1.54	0/*	3.0/0	0/*	1.54	1.50

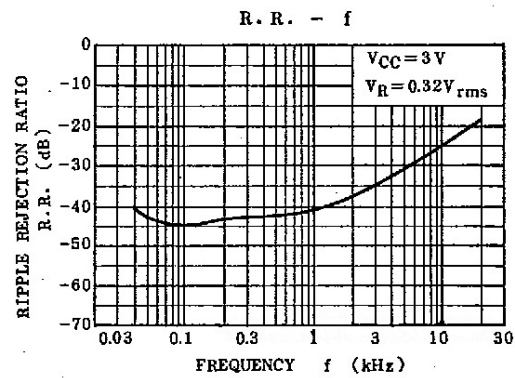
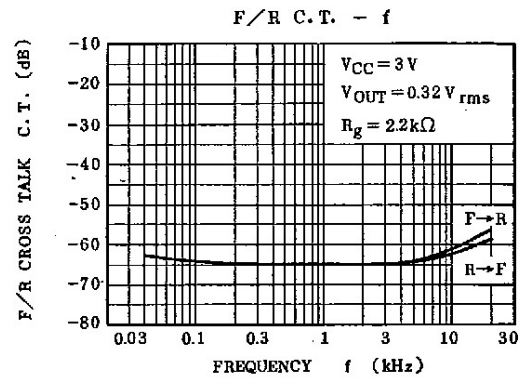
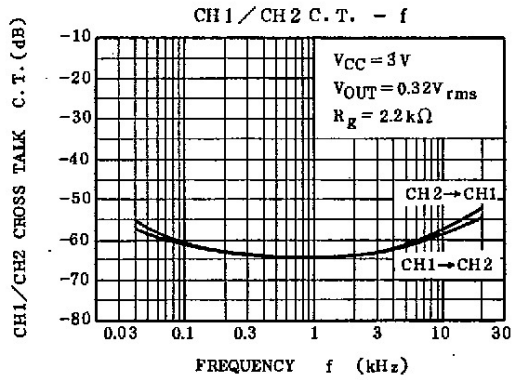
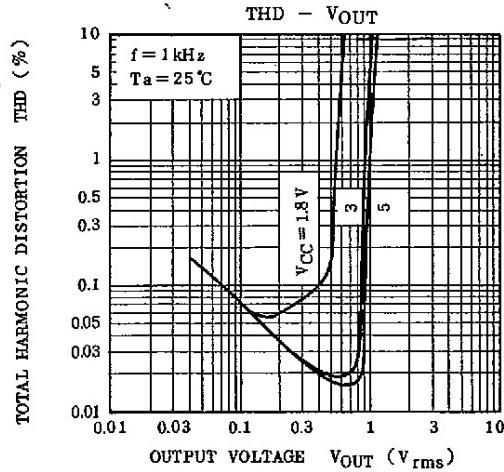
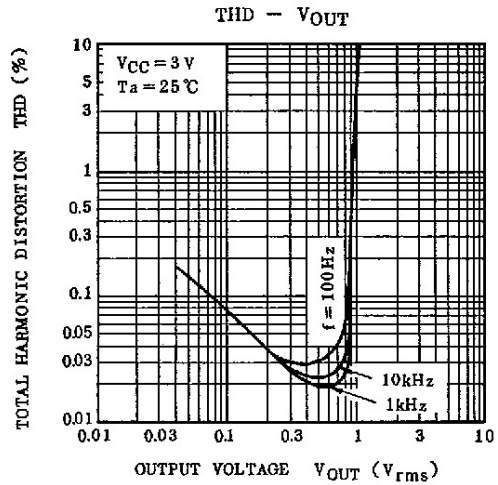
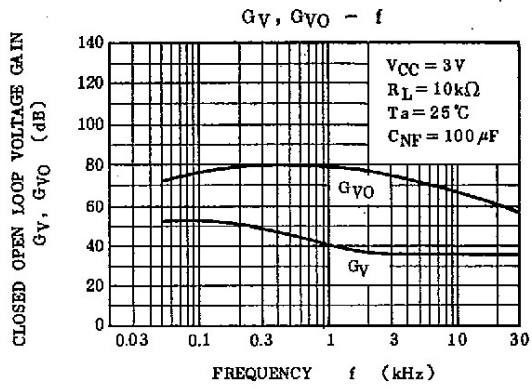
\* : Floating

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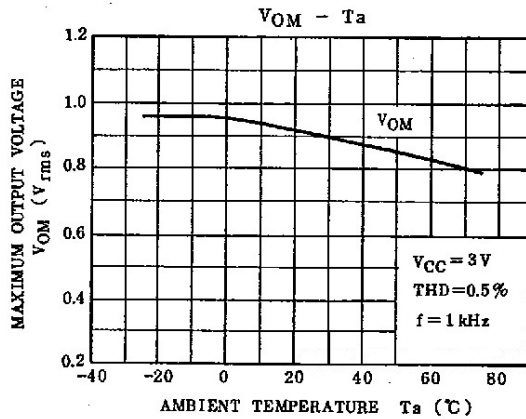
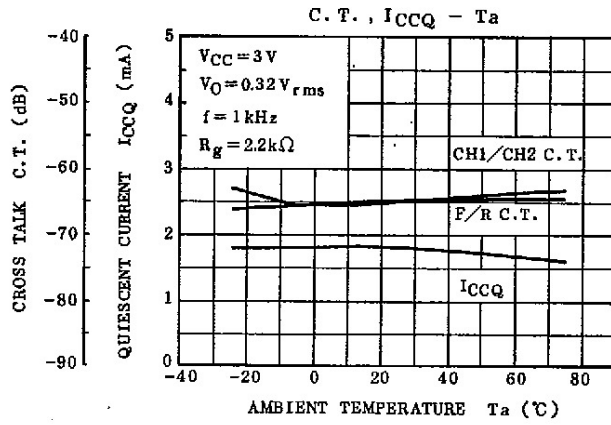
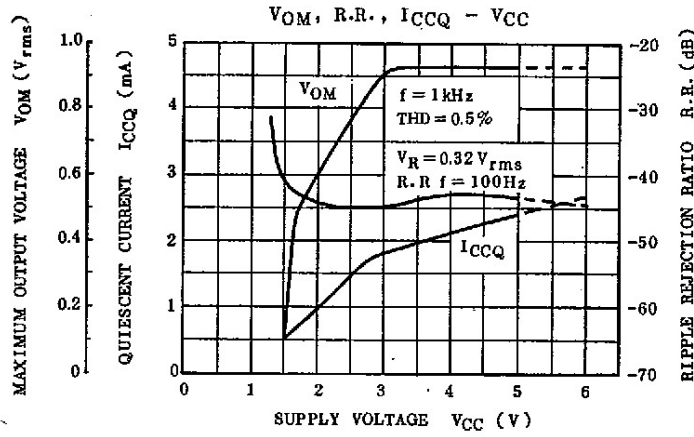
BLOCK DIAGRAM/TEST CIRCUIT



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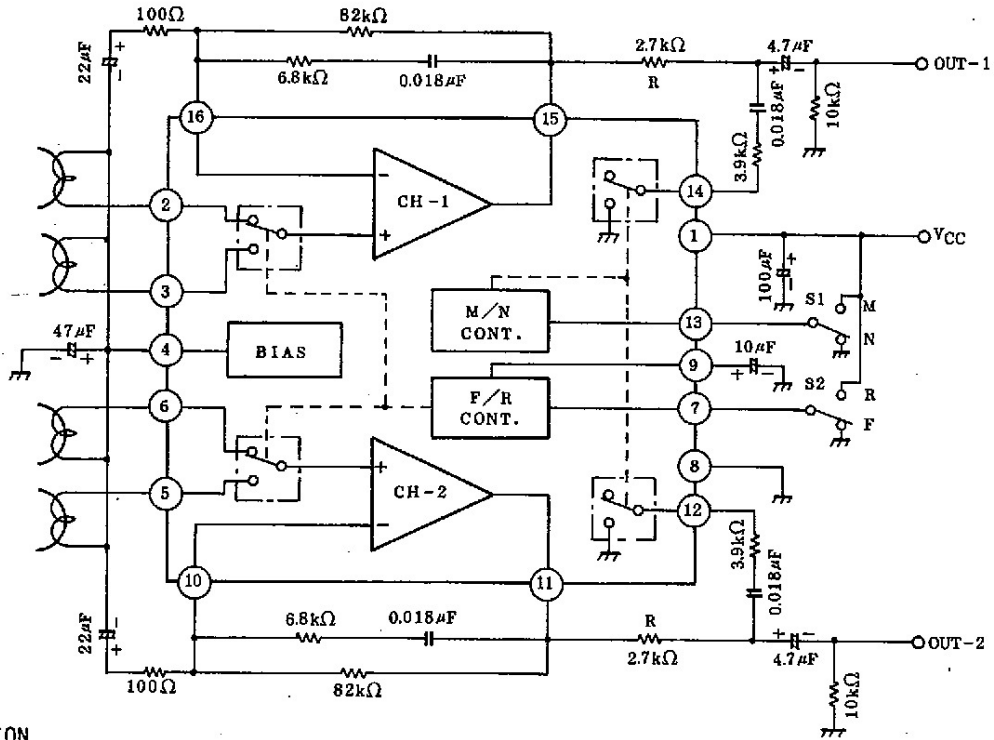


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## APPLICATION CIRCUIT



### CAUTION

- Capacitive load should not be directly connected to output terminal to avoid instable operation.
- When closed loop voltage gain ( $G_V$ ) is set below 40dB, a series resistor more than  $1k\Omega$  connected to the output terminal is needed. Minimum closed loop voltage gain should be more than 21dB.
- About threshold level of S1 and S2, "H" level is above 0.9V, "L" level is below 0.3V.

