

## DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.



TDA8405

# TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH I<sup>2</sup>C BUS CONTROL

## GENERAL DATA

The TDA8405 integrated circuit is a processor for stereo/dual-language signals for stereo-sound television receivers and VTR. The modulated signals at the TDA8405 inputs need to be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The second channel is also modulated with the pilot carrier. The IC is controlled via the two-line, bidirectional I<sup>2</sup>C bus.

## Features

- Amplification of the two a.f. input signals by integrated operational amplifiers.
- Low distortion stereo dematrix
- All operational amplifiers are offset compensated
- I<sup>2</sup>C bus transceiver for system control (port control, mute, mode select, identification, etc.)
- Input port for fast muting
- Two general purpose output ports (three-state, bus-controlled)

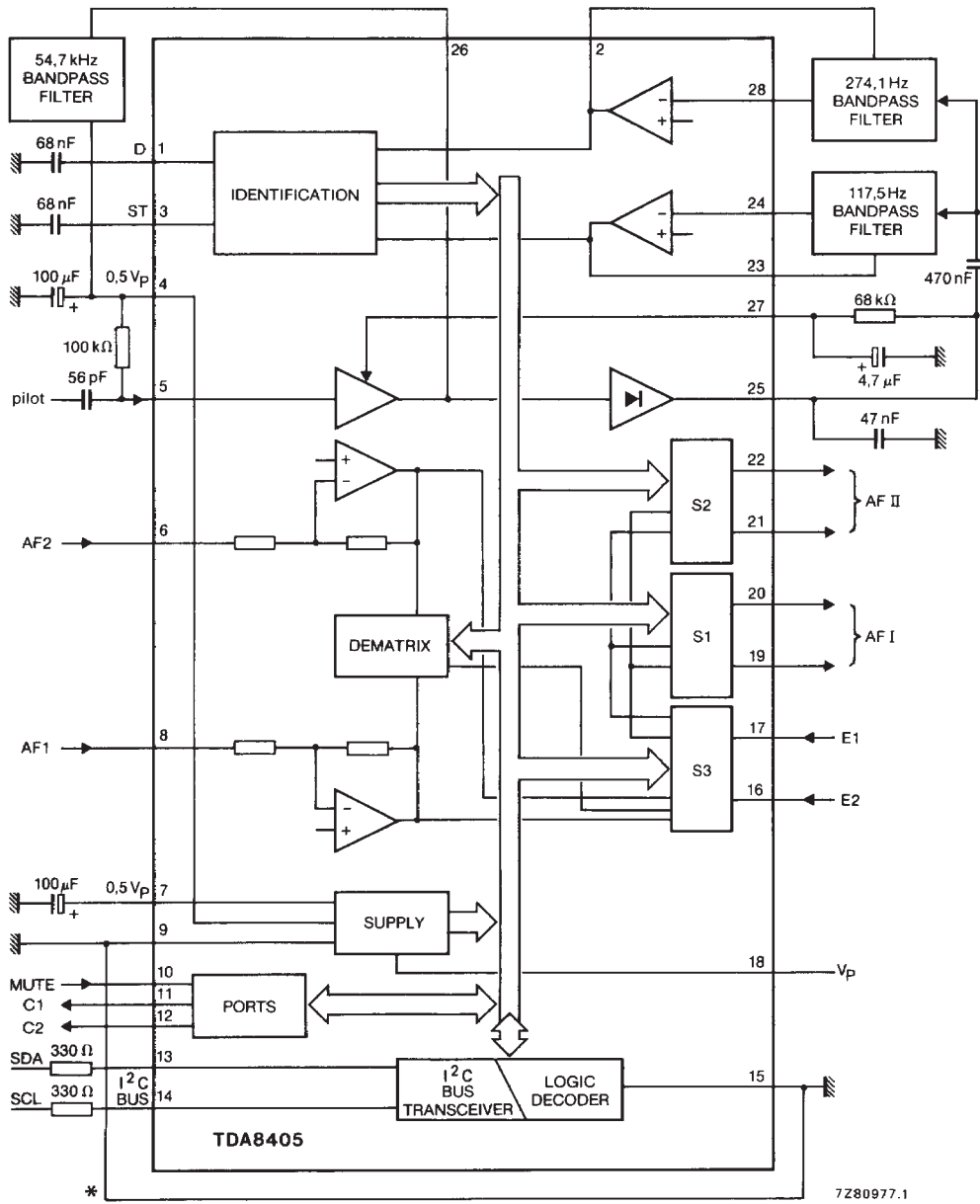
## QUICK REFERENCE DATA

Supply voltage	$V_P = V_{18-9-15}$	typ. 12 V
Supply current	$I_P = I_{18}$	typ. 25 mA
A.F. input signal	$V_{i(rms)} = V_{6-9}, V_{8-9}$	typ. 1 V
Weighted signal-to-noise ratio of the a.f. output-signals (CCIR 468/2)	$(S+N)/N$	$\geq$ 70 dB
Crosstalk attenuation: stereo mode at $f = 1$ kHz	$\alpha_S$	$>$ 40 dB
dual sound mode at $f = 40$ to $12\,500$ Hz	$\alpha_{DS}$	$>$ 70 dB
Pilot signal input sensitivity	$V_i = V_{5-9(rms)}$	typ. 5 mV
Pilot signal amplifier gain control range	$\Delta G_V$	$>$ 40 dB

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

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\* Direct connection between pins 9 and 15 is needed.

Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)*	$V_P = V_{18-9, 15}$	max. 13,2 V
Output current (pins 19, 20, 21, 22)	$I_n$	max. 5 mA
Output current (pins 2, 23)	$I_n$	max. 1 mA
Output current (pins 11, 12)	$I_n$	max. 3 mA
Voltage range at any pin	$V_n$	0 to $V_P$ V
Total power dissipation	$P_{tot}$	max. 1 W
Storage temperature range	$T_{stg}$	-40 to + 150 °C
Operating ambient temperature range	$T_{amb}$	0 to + 70 °C

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\* Supply voltage may be applied only when pins 9 and 15 are connected to ground.

**CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_P = 12\text{ V}$ ;  $V_{i(af)rms} = 1\text{ V}$ ;  $f = 1\text{ kHz}$ ; dematrix aligned;  $V_{ipilot(rms)} = 16\text{ mV}$ ;  
test circuit Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage	$V_P = V_{18-9, 15}$	10,8	12	13,2	V
Supply current at $V_P = 12\text{ V}$	$I_P = I_{18}$	—	25	—	mA
Reference voltage	$V_{ref} = V_{4-9, 15}$	—	$V_P/2$	—	V
DC levels (pins 5, 6, 7, 8, 16, 17, 19, 20, 21, 22, 24, 28)	$V_{n-9, 15}$	—	$V_P/2$	—	V
<b>BUS TRANSCEIVER</b> (pins 13, 14)					
(note 1)					
<b>Clock SCL</b>					
Voltage level LOW	$V_{14-15}$	-0,3	—	1,5	V
Voltage level HIGH	$V_{14-15}$	3,0	—	—	V
Timing LOW period	$t_{PL}$	4,7	—	—	$\mu\text{s}$
Timing HIGH period	$t_{PH}$	4,0	—	—	$\mu\text{s}$
Rise time	$t_r$	—	—	1	$\mu\text{s}$
Fall time	$t_f$	—	—	0,3	$\mu\text{s}$
Input current HIGH	$I_{IH}$	—	—	10	$\mu\text{A}$
Input current LOW	$-I_{IL}$	—	—	10	$\mu\text{A}$
<b>Data</b>					
Voltage level LOW	$V_{13-15}$	-0,3	—	1,5	V
Voltage level HIGH	$V_{13-15}$	3,0	—	—	V
Rise time	$t_r$	—	—	1,0	$\mu\text{s}$
Fall time	$t_f$	—	—	0,3	$\mu\text{s}$
Set-up time data	$t_{SU}$	0,25	—	—	$\mu\text{s}$
Input current HIGH	$I_{13}$	—	—	10	$\mu\text{A}$
Input current LOW	$-I_{13}$	—	—	10	$\mu\text{A}$
Output current LOW	$+I_{13}$	3,0	—	—	mA
<b>MUTE PORT</b> (pin 10) note 2					
Input voltage LOW	$V_{10-15}$	—	—	1,5	V
Input voltage HIGH	$V_{10-15}$	8	—	—	V

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parameter	symbol	min.	typ.	max.	unit
<b>CONTROL PORTS</b> (pins 11, 12)					
3-state HIGH, LOW, high ohmic					
Output resistance in open state	R <sub>11, 12-15</sub>	50	—	—	kΩ
Output voltage LOW	V <sub>11, 12-15</sub>	—	—	0,8	V
Output voltage HIGH	V <sub>11, 12-15</sub>	V <sub>p-1</sub>	—	—	V
Output current LOW	I <sub>11, 12</sub>	500	—	—	μA
Output current HIGH	-I <sub>11, 12</sub>	80	—	—	μA
<b>IDENTIFICATION</b> (See Fig. 3)					
<b>Input amplifier and demodulator</b>					
Input voltage	V <sub>5-9(p-p)</sub>	—	—	2,0	V
Min. input voltage	V <sub>5-9(rms)</sub>	5,0	—	—	mV
Input resistance	R <sub>5-9</sub>	500	—	—	kΩ
Gain	G <sub>25-9</sub>	—	42	—	dB
Gain control range	ΔG	40	—	—	dB
Output voltage (gain-controlled)	V <sub>25-9(p-p)</sub>	—	1,5	—	V
<b>Operational amplifiers</b>					
Input current	I <sub>24, 28</sub>	—	70	—	nA
Gain at f = 200 Hz	G <sub>23-24, G2-28</sub>	78	—	—	dB
Output current	I <sub>2, 23</sub>	1,5	—	—	mA
Output resistance	R <sub>2, 23-9</sub>	—	2	—	kΩ
Output load capacitance	C <sub>2, 23-9</sub>	—	—	30	pF
<b>Schmitt trigger</b>					
A.C. input signal	V <sub>2, 23-9(rms)</sub>	—	1	—	V
Internal discharge resistors	R <sub>1, 3-9</sub>	—	3	—	kΩ
<b>A.F. STAGES</b>					
Input resistance (pins 6, 8, 16 and 17)	R <sub>n-9</sub>	10	—	—	kΩ
Gain (V <sub>19, 20, 21, 22-9</sub> /V <sub>6, 8-9</sub> )	G <sub>1</sub>	—	6	—	dB
Gain (V <sub>19, 20, 21, 22-9</sub> /V <sub>16, 17-9</sub> )	G <sub>2</sub>	—	0	—	dB
Input voltage	V <sub>6, 8-9(rms)</sub>	—	1	—	V
<b>Crosstalk attenuation</b> (notes 3, 4 and 9)					
dual sound	α <sub>DS</sub>	70	—	—	dB
stereo f = 250 Hz to 6,3 kHz	α <sub>S</sub>	40	—	—	dB
stereo f = 40 Hz to 250 Hz; 6,3 kHz to 12,5 kHz	α <sub>S</sub>	30	—	—	dB

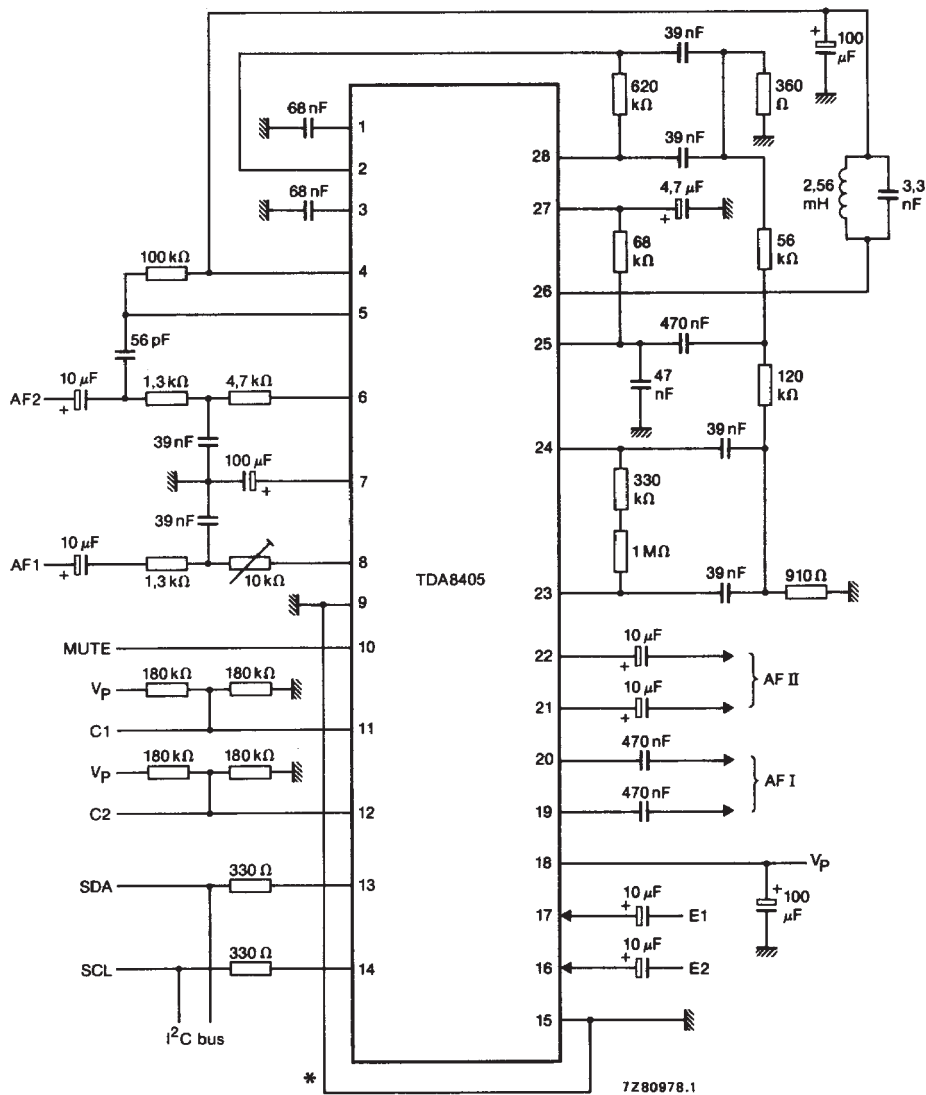
## CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
<b>A.F. STAGES (continued)</b>					
Output resistance	$R_{19,20,21,22}$	—	200	300	$\Omega$
Output load capacitance (pins 19, 20, 21 and 22)	$C_{n-9}$	—	—	1,5	nF
D.C. offsets (note 8) at pins 19, 20, 21 and 22	$\Delta V$	—	—	30	mV
Total harmonic distortion (notes 4 and 5)	THD	—	0,1	0,5	%
Output signal (r.m.s. value) (pins 19, 20, 21 and 22)	$V_{n-9(rms)}$	—	—	2,0	V
Ripple rejection (note 6)	RR	30	35	—	dB
Noise rejection (note 7) (noise from I <sup>2</sup> C bus)	NR	80	—	—	dB
Signal-to-noise ratio (note 7)	(S+N)/N	70	—	—	dB
Ident signal suppression		70	—	—	dB
Signal suppression during mute (notes 4 and 7)		70	—	—	dB

## Notes to the characteristics

1. Full specification of the I<sup>2</sup>C bus will be supplied on request.
2. Programmable mute state. If the SC3 bit in the I<sup>2</sup>C bus is LOW then the mute input is active LOW; if the mute bit is set to HIGH then the mute input is active HIGH.
3. Crosstalk attenuation definition:  $20 \log$  (unwanted output signal/input signal).
4. Frequency range:  $40 \text{ Hz} < f < 12,5 \text{ kHz}$ .
5. In dual sound mode.
6. Test circuit as in Fig. 4: ripple rejection = output modulation due to hum on the supply line.
7. Related to 2 V (r.m.s.) output signal at pin 19, 20, 21 or 22; noise weighted according to CCIR 468/2.
8. Caused by any change of the switch position.
9.  $\alpha_5$  measured without de-emphasis network.

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\* Direct connection between pins 9 and 15 is needed.

Fig. 2 Test circuit.

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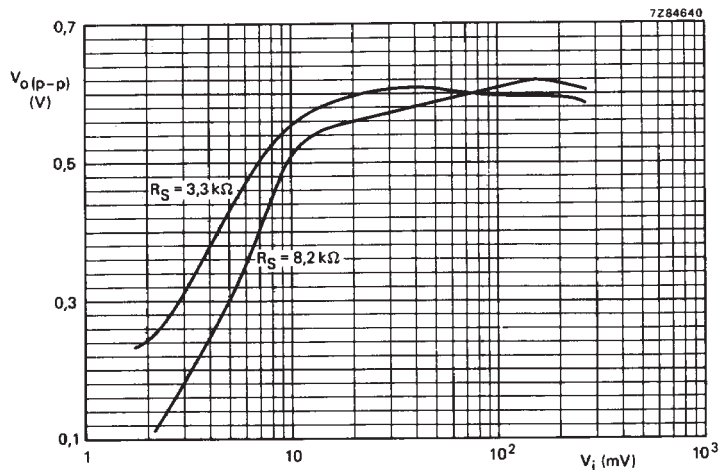


Fig. 3 Controlled output voltage as a function of the input signal ( $Q = 80$ ); pilot frequency  $f_0 = 54$  kHz;  $R_S$  = source resistance.

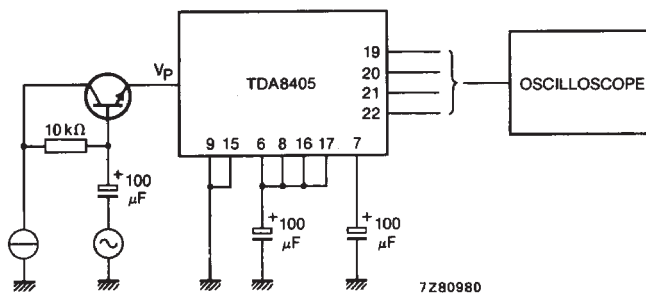


Fig. 4 Test circuit for ripple rejection: supply (d.c.) + pulse (r.m.s.) voltage at 100 Hz = 12 V + 50 mV.



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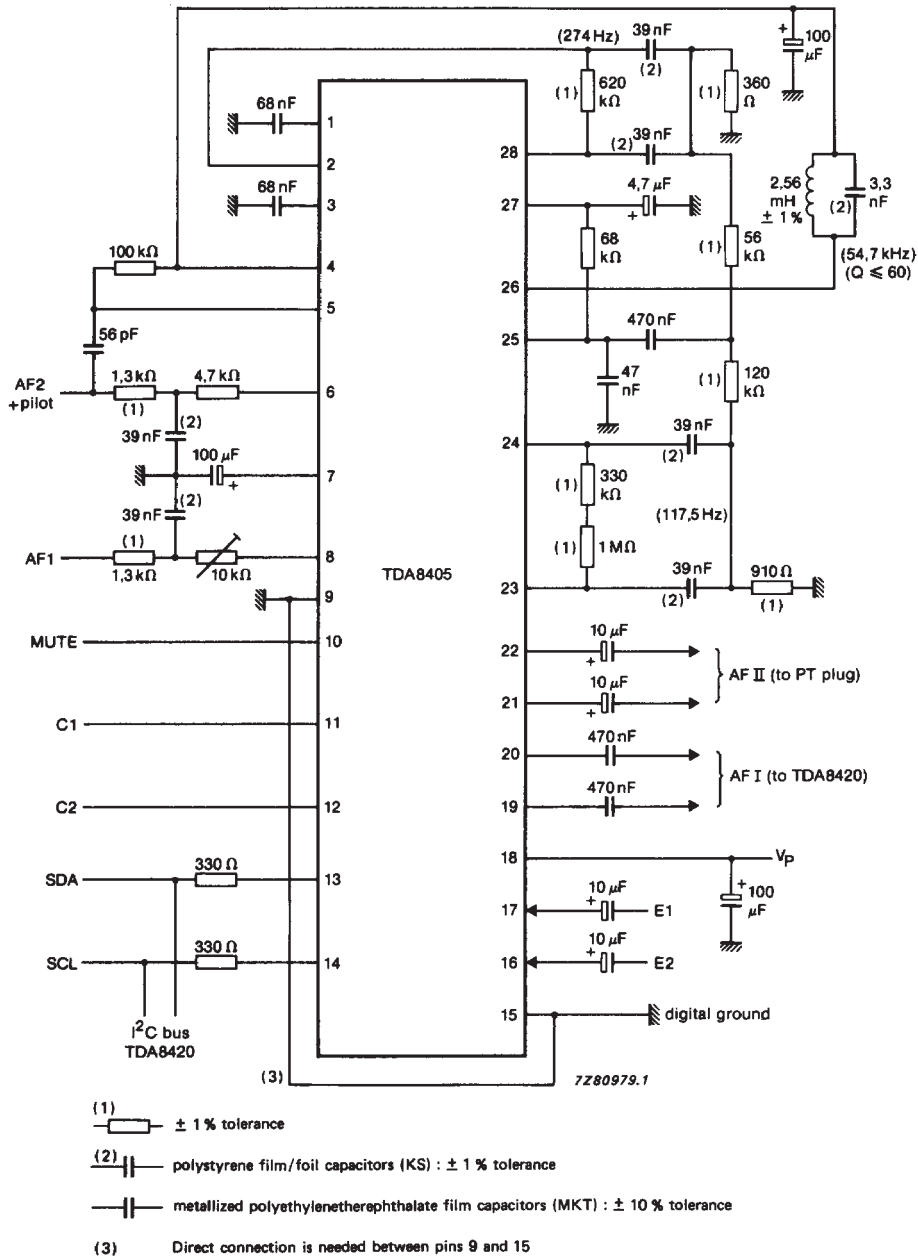


Fig. 5 Application diagram.