Philips Semiconductors

Data sheet	
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TDA4660

64 μs baseband delay line

FEATURES

- Two comb filters using the switched-capacitor technique and with a delay time of 64 μs
- Generation of a 3 MHz internal clock that is line-locked via the sandcastle pulse

GENERAL DESCRIPTION

The TDA4660 is an integrated baseband delay line circuit. It provides a delay of 64 μs for the colour difference signals, −(R-Y) and −(B-Y), in multi-standard TVs.

The colour difference signals are AC-coupled to pins 16 and 14 respectively and clamped at the input stages. The signals are then fed via buffers to the delay line circuit. The delay line circuit is driven by a 3 MHz internal clock which enables the circuit to produce the required delay of 64 μs.

The outputs from the delay line circuit are fed through sample-and-hold and low-pass filters to suppress the clock signal. The delayed and non-delayed signals are then added and fed to the output pins, 11 and 12, via buffers.

The internal clock is derived from a 6 MHz voltage controlled oscillator (VCO) which is line-locked via a PLL to the sandcastle pulse at pin 5.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{1-3}	digital supply voltage		5.3	-	6.0	V
V_{9-10}	analog supply voltage		5.3	-	6.0	V
I_1	digital supply current		-	1.0	2.0	mA
I_9	analog supply current		-	4.5	8.0	mA
Colour difference input signals PAL and NTSC						
V_{16-10}	−(R-Y) (peak-to-peak value)		-	0.525	-	V
V_{14-10}	−(B-Y) (peak-to-peak value)		-	0.675	-	V
SECAM						
V_{16-10}	−(R-Y) (peak-to-peak value)	note 1	-	1.05	-	V
V_{14-10}	−(B-Y) (peak-to-peak value)	note 1	-	1.35	-	V
Gain of colour difference output signals (V_O/V_I)						
V_{11}/V_{16}	PAL, NTSC		4.5	5.5	6.5	dB
V_{12}/V_{14}			4.5	5.5	6.5	dB
V_{11}/V_{16}	SECAM	note 1	−1.5	−0.5	0.5	dB
V_{12}/V_{14}		note 1	−1.5	−0.5	0.5	dB

Note to the quick reference data

1. The signals must be blanked line-sequentially. The blanking levels must be equal to the uncoloured signal.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4660	16	DIL	plastic	SOT38
TDA4660T	16	SO16L	plastic	SOT162A

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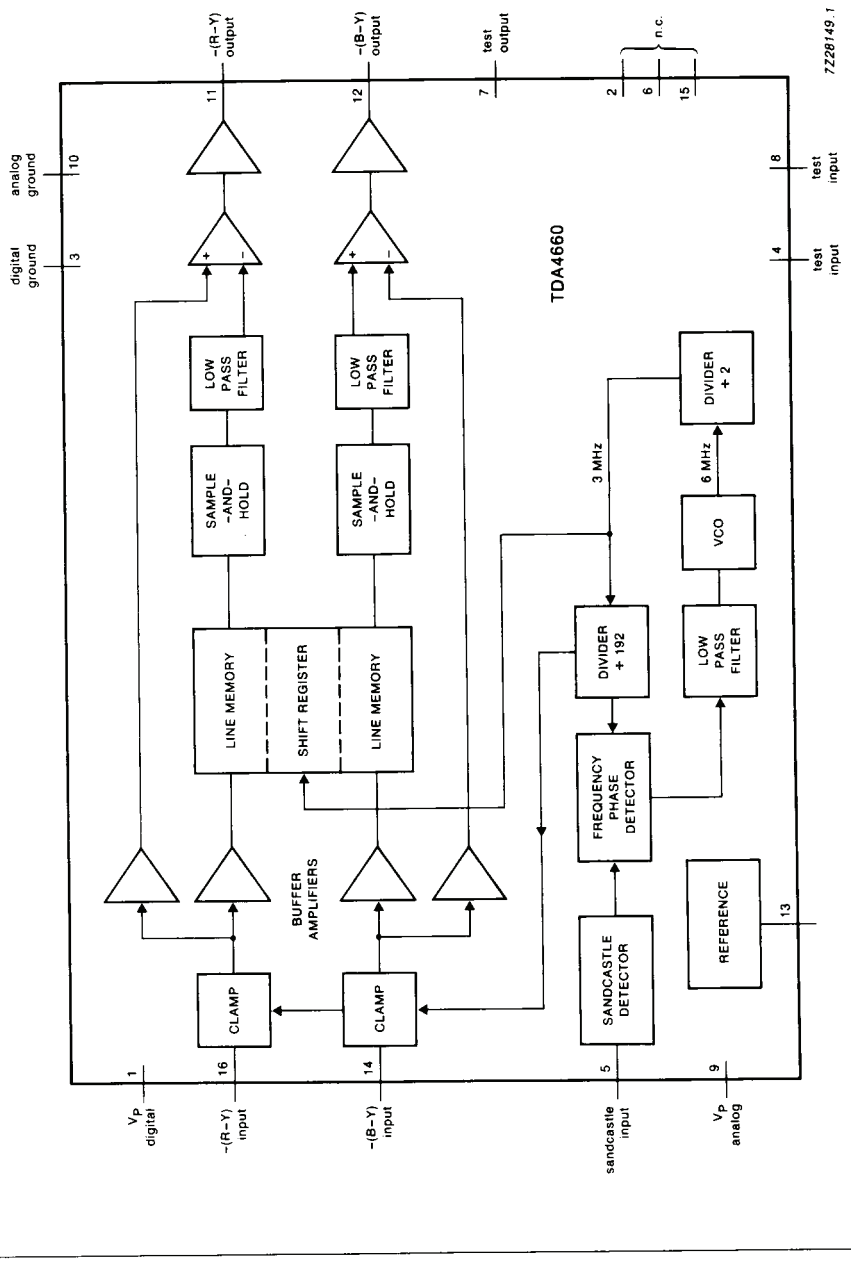

Fig.1 Block diagram.

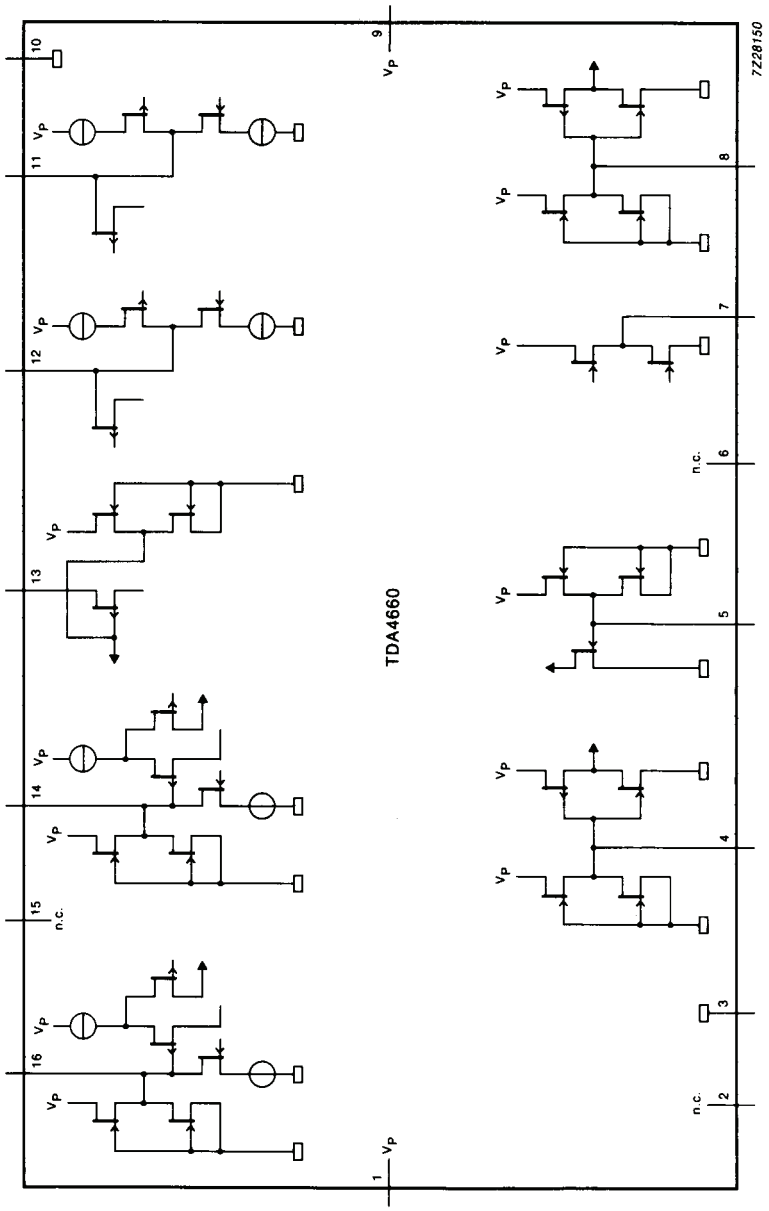

Fig.2 Internal pin circuit diagram.

PINNING

PIN	DESCRIPTION
1	digital supply voltage
2	not connected
3	digital ground
4	test input
5	sandcastle input
6	not connected
7	test output
8	test input
9	analog supply voltage
10	analog ground
11	-(R-Y) output
12	-(B-Y) output
13	reference current
14	-(B-Y) input
15	not connected
16	-(R-Y) input

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{1-3}, V_{9-10}	supply voltages		−0.5	+ 7	V
V_{n-3}, V_{n-10}	voltage at pins 4, 5, 7, 8, 11, 12, 14 and 16		−0.5	+ 7	V
T_{amb}	operating ambient temperature range		0	+ 70	°C
T_{stg}	storage temperature range		−25	+ 150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j-a}$	from junction to ambient in free air	-	80	K/W

CHARACTERISTICS

V_P = 5.6 V; f_H = 15.625 kHz; T_{amb} = 25 °C; R13 = 1 MΩ, C13 = 10 nF (see Fig.3); nominal signal for 75% colour bars; sandcastle with burst-key-pulse; supply voltages, digital and analog, must be connected; (see Fig.3); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{1-3}	digital supply voltage		5.3	5.6	6.0	V
V_{9-10}	analog supply voltage		5.3	5.6	6.0	V
I_1	digital supply current		-	1	2	mA
I_9	analog supply current		-	4.5	8	mA
P_{tot}	total power dissipation		-	31	60	mW
Colour difference input signals PAL, NTSC						
$V_{16(p-p)}$	−(R-Y) input signal (peak-to-peak value)		-	0.525	-	V
$V_{14(p-p)}$	−(B-Y) input signal (peak-to-peak value)		-	0.675	-	V
$V_{14,16(p-p)}$	maximum symmetrical input signal (peak-to-peak value)	before clipping	1	-	-	V
SECAM (note 1)						
$V_{16(p-p)}$	−(R-Y) input signal (peak-to-peak value)		-	1.05	-	V
$V_{14(p-p)}$	−(B-Y) input signal (peak-to-peak value)		-	1.33	-	V
$V_{14,16(p-p)}$	maximum symmetrical input signal (peak-to-peak value)	before clipping	2	-	-	V
C14, C16	input capacitance		-	-	10	pF
R14, R16	input resistance during clamping		-	-	40	kΩ
$V_{14,16-10}$	clamping voltage	proportional to V_P	1.55	1.65	1.75	V
Sandcastle pulse (note 2)						
I_5	input leakage current		-	-	10	µA
C5	input capacitance		-	-	10	pF
V_{se}	slicing level below top sync level		-	1.5	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{bk}	input frequency of burst key		14.2	15.6	17	kHz
V_5	top sync pulse		3	-	7	V
Delayed colour difference output signals						
	amplitude ratio V_{11}/V_{16}, V_{12}/V_{14}	PAL, NTSC	4.5	5.5	6.5	dB
		SECAM	−1.5	−0.5	+ 0.5	dB
V_{11}/V_{12}	ratio of output amplitudes for equal input signals	$V_{14,16(p-p)}$ = 1.35 V	−0.4	0	+ 0.4	dB
t_d	time difference between non-delayed and delayed signals		63.94	64	64.06	μs
t_{ud}	delay time for non-delayed signal pulse response	$V_{14,16(p-p)}$ = 1.35 V	-	85	-	ns
t_{rud}	output transient time of; undelayed signal V_{11} and V_{12}	transient = 300 μs; SECAM mode	*	320	*	ns
t_{rd}	delayed signal V_{11} and V_{12}		*	350	*	ns
V_{11n}/V_{11n+1} V_{12n}/V_{12n+1}	ratio of the output signal for adjacent time samples at constant input signal	$V_{11,12(p-p)}$ = 1.35 V; SECAM mode	−0.1	0	+ 0.1	dB
V_{11}, V_{12}	noise voltage (RMS value)	V_{16-10}, V_{14-10} = 0 V; R_S = 300 Ω (source); f = 10 kHz to 1 MHz	-	-	1.2	mV
R11, R12	output resistance		-	330	400	Ω
V_{11}, V_{12}	DC output voltage	proportional to V_P	2.9	3.1	3.3	V

Notes to the characteristics

1. The signals must be blanked line-sequentially. The blanking levels must be equal to the uncoloured signal.
2. The leading edge of the burst key is used for timing.

* Value to be fixed.

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APPLICATION INFORMATION

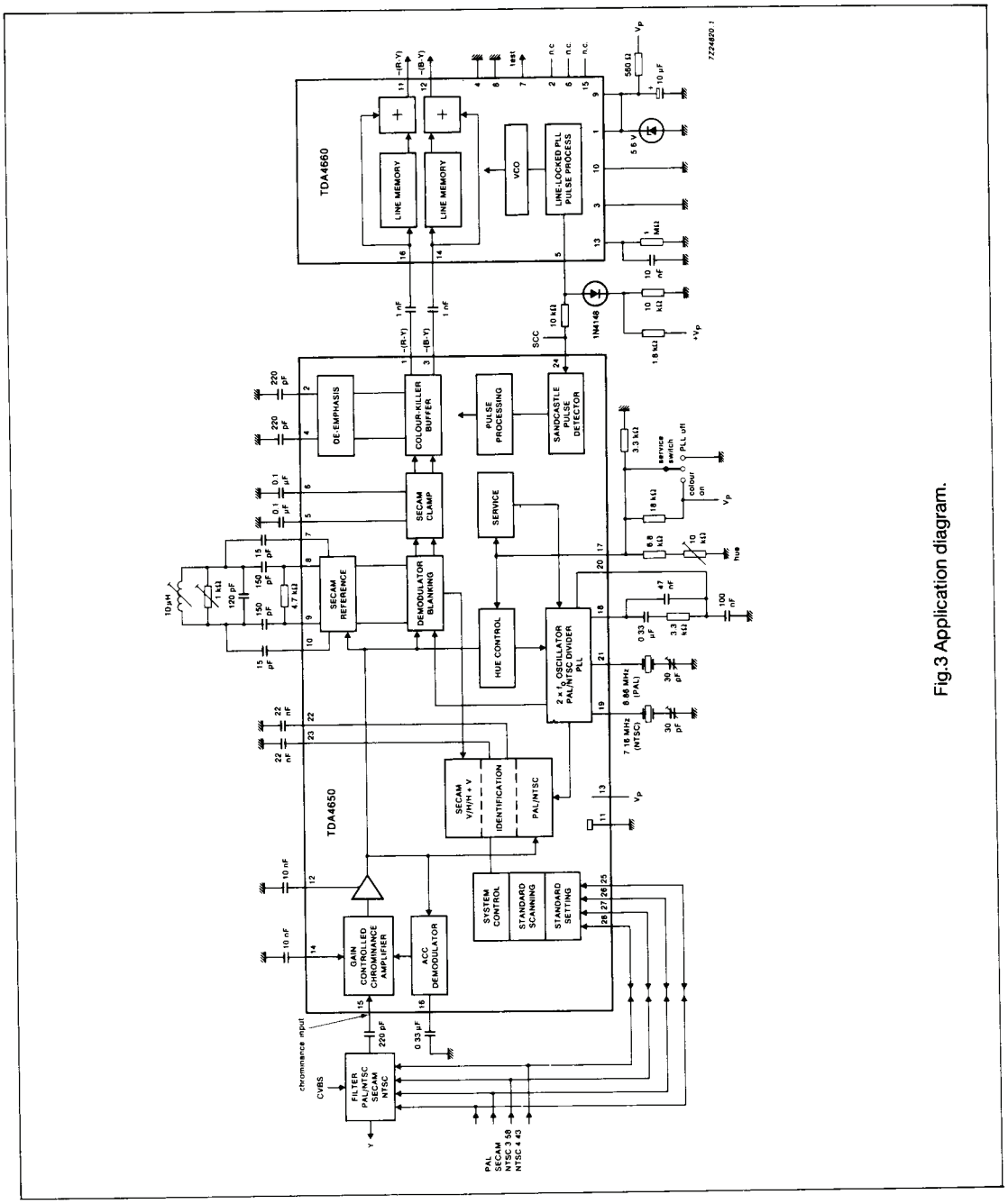

Fig.3 Application diagram.