

# 74199 Shift Register

8-Bit Parallel-Access Shift Register  
Product Specification

## Logic Products

### FEATURES

- Buffered clock and control inputs
  - Shift right and parallel load capability
  - Fully synchronous data transfers
  - J-K̄ (D) inputs to first stage
  - Clock enable for hold (do nothing) mode
  - Asynchronous Master Reset
- ### DESCRIPTION

The functional characteristics of the '199 8-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT
74199	35MHz	90mA

### ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74199N

#### NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

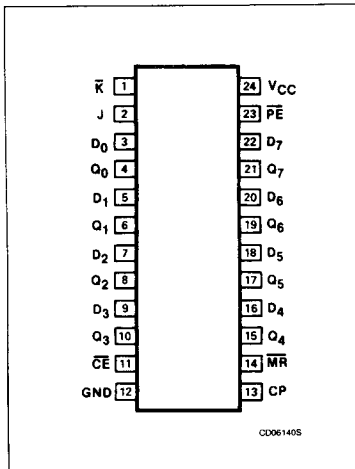
### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1ul
$Q_0 - Q_7$	Parallel outputs	10ul

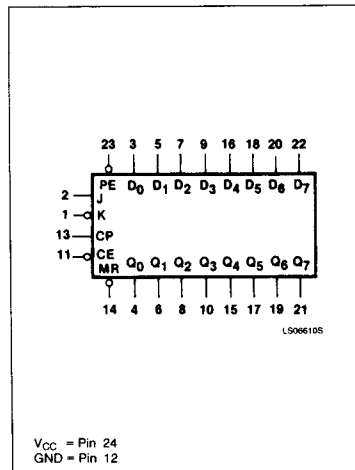
#### NOTE:

A 74 unit load (ul) is understood to be  $40\mu A$   $I_{IH}$  AND  $-1.6mA$   $I_{IL}$ .

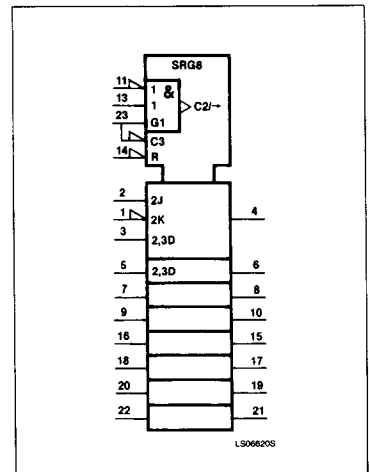
### PIN CONFIGURATION



### LOGIC SYMBOL



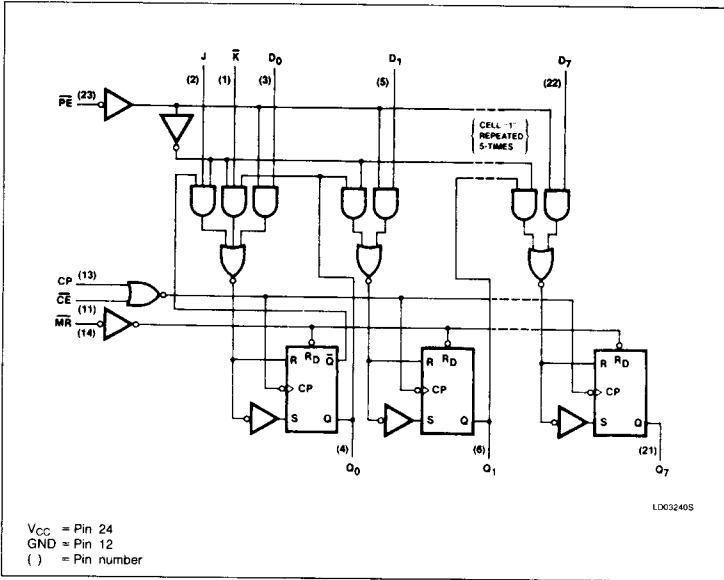
### LOGIC SYMBOL (IEEE/IEC)



# Shift Register

74199

## LOGIC DIAGRAM



The '199 operates in two primary modes: shift right ( $Q_0 \rightarrow Q_1$ ) and parallel load, which are controlled by the state of the Parallel Enable ( $\overline{PE}$ ) input. Serial data enters the first flip-flop ( $Q_0$ ) via the J and  $\overline{K}$  inputs when the  $\overline{PE}$  input is HIGH, and is shifted one bit in the direction  $Q_0 \rightarrow Q_1 \rightarrow Q_2$  following each LOW-to-HIGH clock transition. The J and  $\overline{K}$  inputs provide the flexibility of the J-K type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as eight common clocked D flip-flops when the  $\overline{PE}$  input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ( $D_0 - D_7$ ) is transferred to the respective  $Q_0 - Q_7$  outputs.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The '199 utilizes edge-triggering, therefore, there is no restriction on the activity of the J,  $\overline{K}$ ,  $D_n$ , and  $\overline{PE}$  inputs for logic operation, other than the set-up and release time requirements.

The clock input is a gated OR structure which allows one input to be used as an active-LOW Clock Enable ( $\overline{CE}$ ) input. The pin assignment for the CP and  $\overline{CE}$  inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of  $\overline{CE}$  input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

## MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS							
	$\overline{MR}$	CP	$\overline{CE}$	PE	J	$\overline{K}$	$D_n$	$Q_0$	$Q_1$	.....	$Q_6$	$Q_7$			
Reset (clear)	L	X	X	X	X	X	X	L	L	.....	L	L			
Shift, set first stage	H	$\uparrow$	l	h	h	h	X	H	$q_0$	.....	$q_5$	$q_6$			
Shift, reset first stage	H	$\uparrow$	l	h	l	l	X	L	$q_0$	.....	$q_5$	$q_6$			
Shift, toggle first stage	H	$\uparrow$	l	h	h	l	X	$\overline{q_0}$	$q_0$	.....	$q_5$	$q_6$			
Shift, retain first stage	H	$\uparrow$	l	h	l	h	X	$q_0$	$q_0$	.....	$q_5$	$Q_6$			
Parallel load	H	$\uparrow$	l	l	X	X	$d_n$	$d_0$	$d_1$	.....	$d_6$	$d_7$			
Hold (do nothing)	H	$\uparrow$	$h^{(a)}$	X	X	X	X	$q_0$	$q_1$	.....	$q_6$	$q_7$			

H = HIGH voltage level steady state.

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.

L = LOW voltage level steady state.

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

X = Don't care

$d_n(q_n)$  = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.

$\uparrow$  = LOW-to-HIGH clock transition.

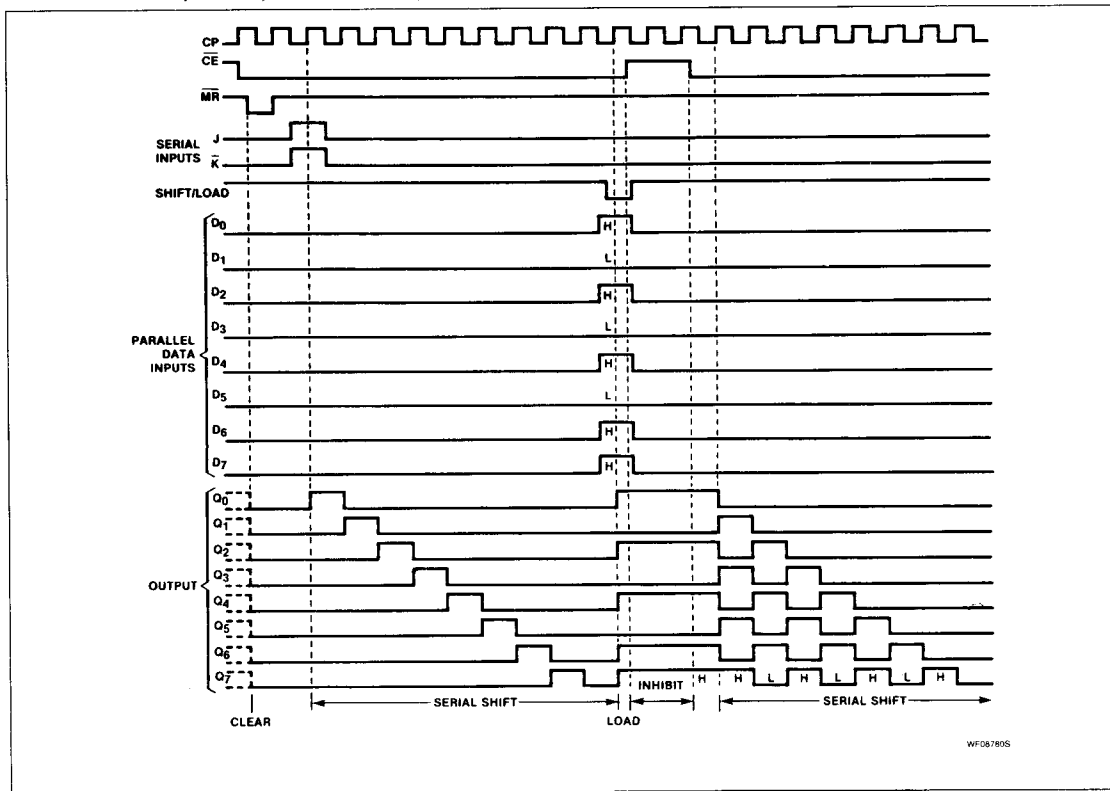
**NOTE:**

a. The LOW-to-HIGH transition of  $\overline{CE}$  should only occur while CP is HIGH for conventional operation.

# Shift Register

74199

## TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



5

### ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V <sub>CC</sub>	Supply voltage	7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +5.5	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in HIGH output state	-0.5 to +V <sub>CC</sub>	V
T <sub>A</sub>	Operating free-air temperature range	0 to 70	°C

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V <sub>CC</sub>	4.75	5.0	5.25	V
V <sub>IH</sub>	2.0			V
V <sub>IL</sub>			+0.8	V
I <sub>IK</sub>			-12	mA
I <sub>OH</sub>			-800	V
I <sub>OL</sub>			16	mA
T <sub>A</sub>	0		70	°C

## Shift Register

74199

**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS <sup>1</sup>	74199			UNIT
		Min	Typ <sup>2</sup>	Max	
V <sub>OH</sub> HIGH-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OH</sub> = MAX	2.4	3.4		V
V <sub>OL</sub> LOW-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OL</sub> = MAX		0.2	0.4	V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-1.5	V
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V			1.0	mA
I <sub>IH</sub> HIGH-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4V			40	μA
I <sub>IL</sub> LOW-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4V			-1.6	mA
I <sub>OS</sub> Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-18		-57	mA
I <sub>CC</sub> Supply current <sup>4</sup> (total)	V <sub>CC</sub> = MAX		90	127	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- I<sub>OS</sub> is tested with V<sub>OUT</sub> = ± 0.5V and V<sub>CC</sub> = V<sub>CC</sub> MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I<sub>CC</sub> with  $\bar{K}$ , J and D inputs at 4.5V, momentary ground clock, then apply 4.5V, ground  $\bar{CE}$ ,  $\bar{MR}$  and  $\bar{PE}$ .

**AC ELECTRICAL CHARACTERISTICS** T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C <sub>L</sub> = 15pF, R <sub>L</sub> = 400Ω		
		Min	Max	
f <sub>MAX</sub> Maximum clock frequency	Waveform 1	25		MHz
t <sub>PLH</sub> Propagation delay t <sub>PHL</sub> Clock to output	Waveform 1		26 30	ns
t <sub>PHL</sub> Propagation delay $\bar{MR}$ to output	Waveform 2		35	ns

Per industry convention, f<sub>MAX</sub> is the worst case of the maximum device operating frequency with no constraints on t<sub>r</sub>, t<sub>f</sub>, pulse width or duty cycle.

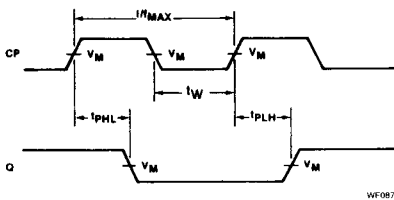
**AC SET-UP REQUIREMENTS** T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t <sub>w</sub> Clock pulse width	Waveform 1	20		ns
t <sub>w</sub> $\bar{MR}$ pulse width	Waveform 2	20		ns
t <sub>s</sub> Set-up time, J, $\bar{K}$ and data to clock	Waveform 3	20		ns
t <sub>h</sub> Hold time, J, $\bar{K}$ and data to clock	Waveform 3	0		ns
t <sub>s</sub> Set-up time, $\bar{CE}$ to clock	Waveform 3	30		ns
t <sub>h</sub> Hold time, $\bar{CE}$ to clock	Waveform 3	0		ns
t <sub>s</sub> Set-up time, $\bar{PE}$ to clock	Waveform 3	30		ns
t <sub>h</sub> Hold time, $\bar{PE}$ to clock	Waveform 3	0		ns
t <sub>rec</sub> Recovery time, $\bar{MR}$ to clock	Waveform 2	30		ns

# Shift Register

74199

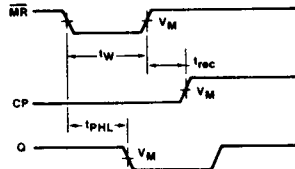
## AC WAVEFORMS



WF08790S

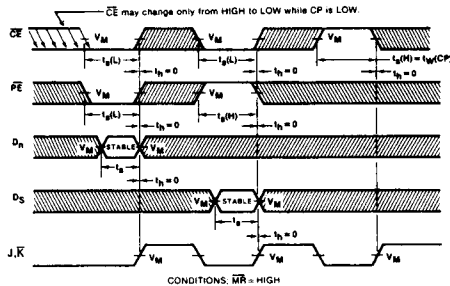
The number of clock pulses required between the  $t_{PLH}$  and  $t_{PHL}$  measurements can be determined from the appropriate Truth Tables.

**Waveform 1. Clock To Output Delays And Clock Pulse Width**



WF08600S

**Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time**



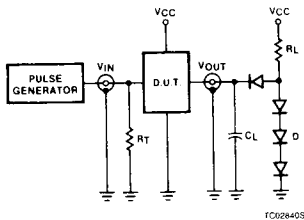
WF08810S

For all waveforms,  $V_M = 1.5V$  for 74 and 74S;  $V_M = 1.3V$  for 74LS.  
The shaded areas indicate when the input is permitted to change for predictable performances.

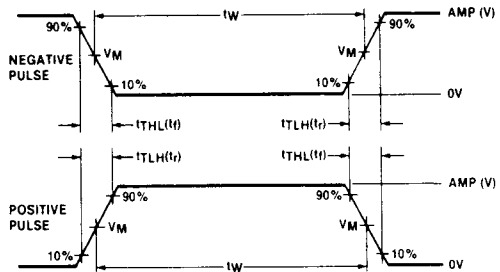
**Waveform 3**

5

## TEST CIRCUITS AND WAVEFORMS



TC02840S



WF06450S

$V_M = 1.3V$  for 74LS;  $V_M = 1.5V$  for all other TTL families.

### Test Circuit For 74 Totem-Pole Outputs

#### DEFINITIONS

$R_L$  = Load resistor to  $V_{CC}$ ; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$t_{TLH}$ ,  $t_{THL}$  Values should be less than or equal to the table entries.

### Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	$t_{TLH}$	$t_{THL}$
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns